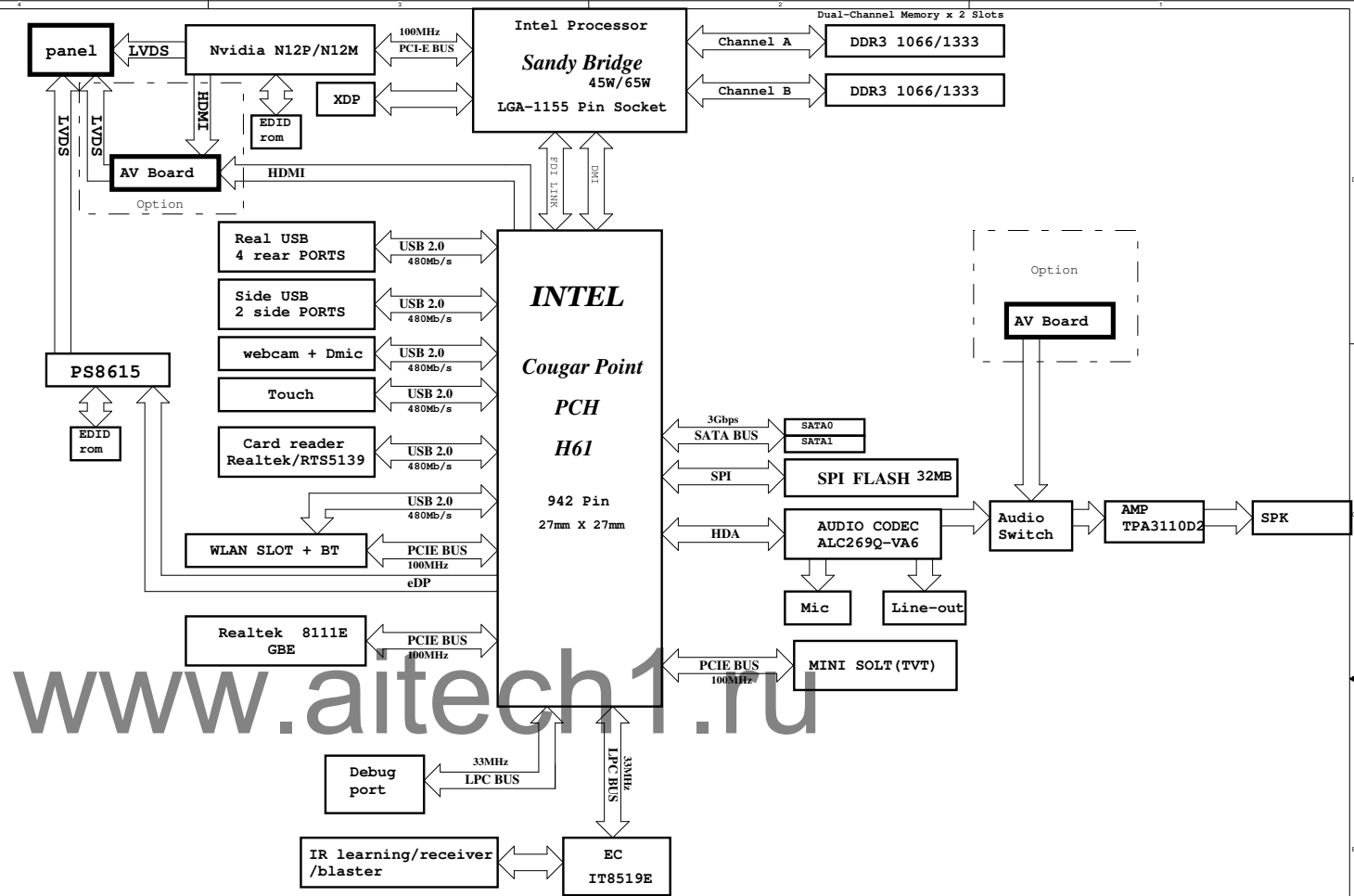
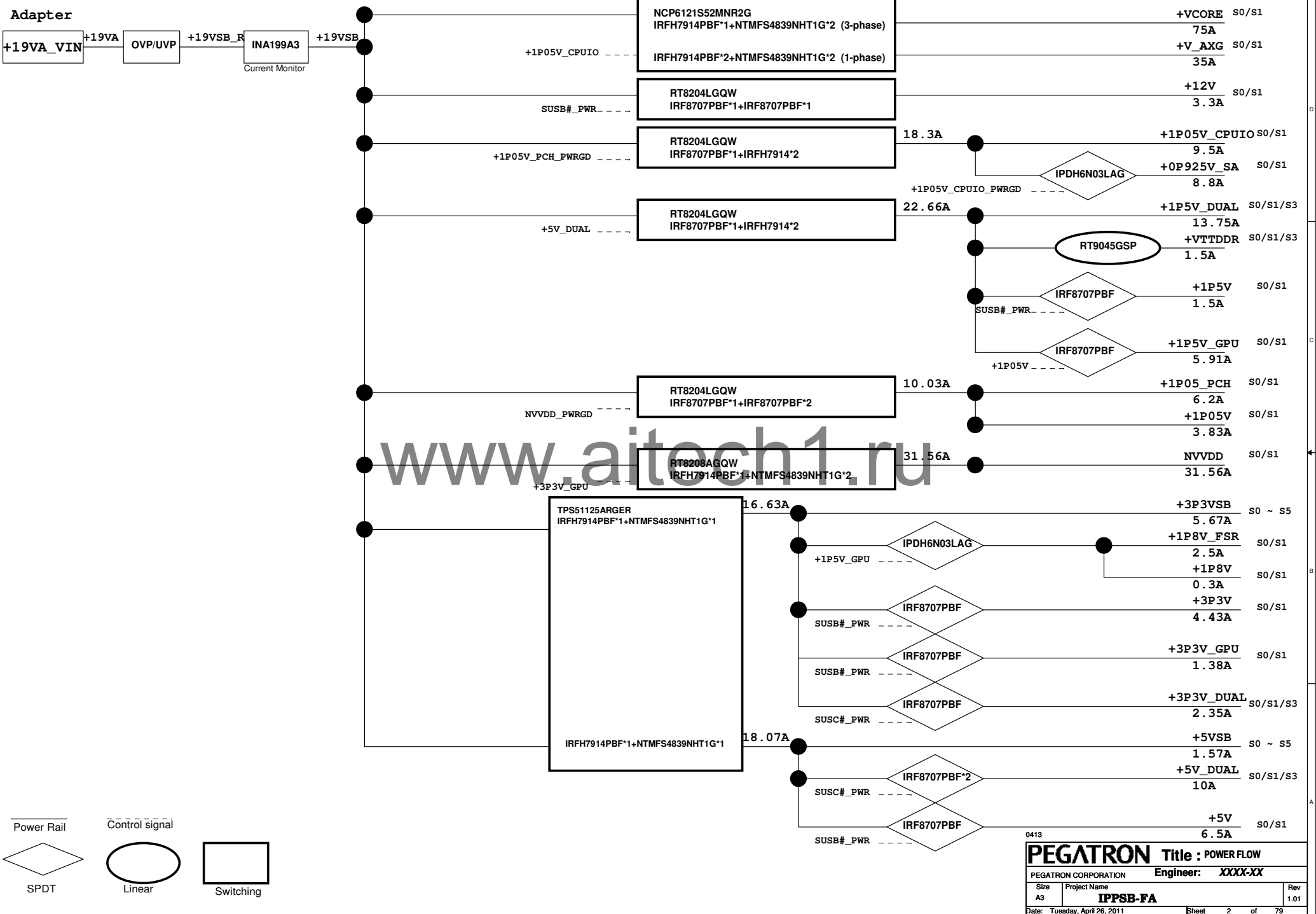
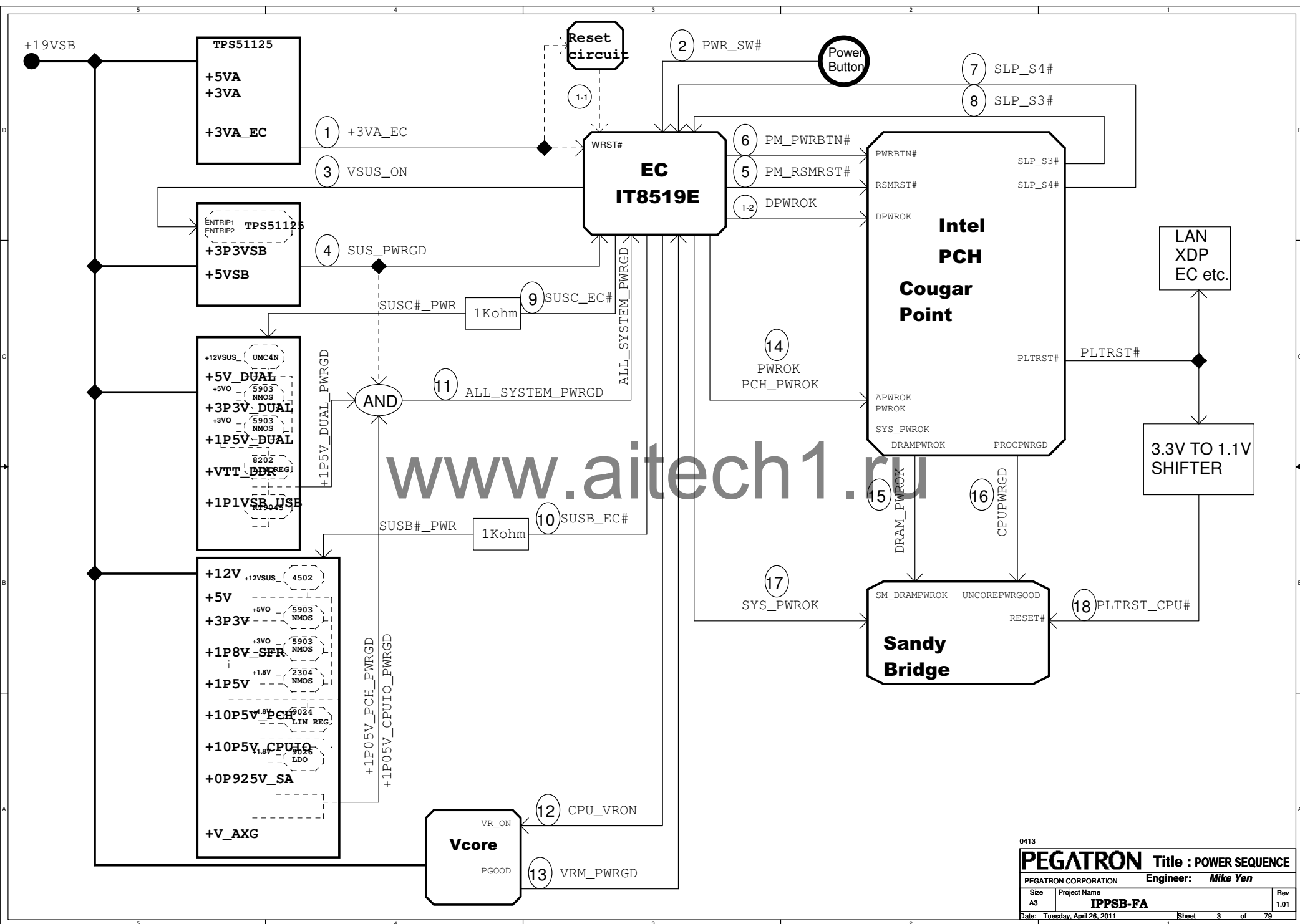


IPPSB-FA

PAGE	TITLE
01	BLOCK DIAGRAM
02	POWER FLOW
03	POWER SEQUENCE
04-09	CPU LGA1155 DDR3 A 1-6
10	DDR3 CHANNEL A G/F
11	DDR3 CHANNEL B G/F
12	DDR3 TERMINATION A&B
13	PLTRST_CPU# & SMBus
14	Converter Controller
15-16	LVDS&AV CONN
17-25	INTEL PCH 1-9
27-28	LAN
29-30	CODEC&CONN
31-32	AMP&SWITCH
33-35	USB&HUB&BT
36	HPD DET
37-38	MINI CARD (WL&TVT&DMC)
39	Misc. conn&Touch&Wcam&RTC
40	FAN
41	PWR LED & Button*
42	IR LEDs
43-44	EC 8519
45	SM BUS & SPI ROM
46	SCREW HOLE
47	UVP, OVP & +19VSB
48	LOAD SWITCH
49	+3P3VSB&+5VSB
50	+1P5V_DUAL & +1P2V
51	Current Monitor
52	+12V & +1P8V
53	+1P05V_CPUIO&+0P925V_SA
54	POWER_PROTECT
55	+1P05V_CPUIO CAP
56	+VTT_DDR
57	+V_AXG DRIVER
58	+VCORE CONTROLLER
59-61	+VCORE CAP
62	+1P05V&+1P05V_PCH
63-64	CPU&PCH XDP DEBUG CONNECTOR
65	VGA CONN
66-67	GPU DDR3
68	VGA-N12P_STRAPPING+EEPROM
69	MXM.VGA-N12P_Xtal/Thermal
70-71	GPU HDMI (DMC&AV)
72	GPU CTRL
73	GPU.VGA_N12P_PCI-E I/F
74	GPU PCI-E LVDS_VGA
75	MXM.GPU Discharge
76	GPU_POWER&GND
77	MXM.NVVD
78	Card Reader RTS5139-GR
79	EDP CH7511

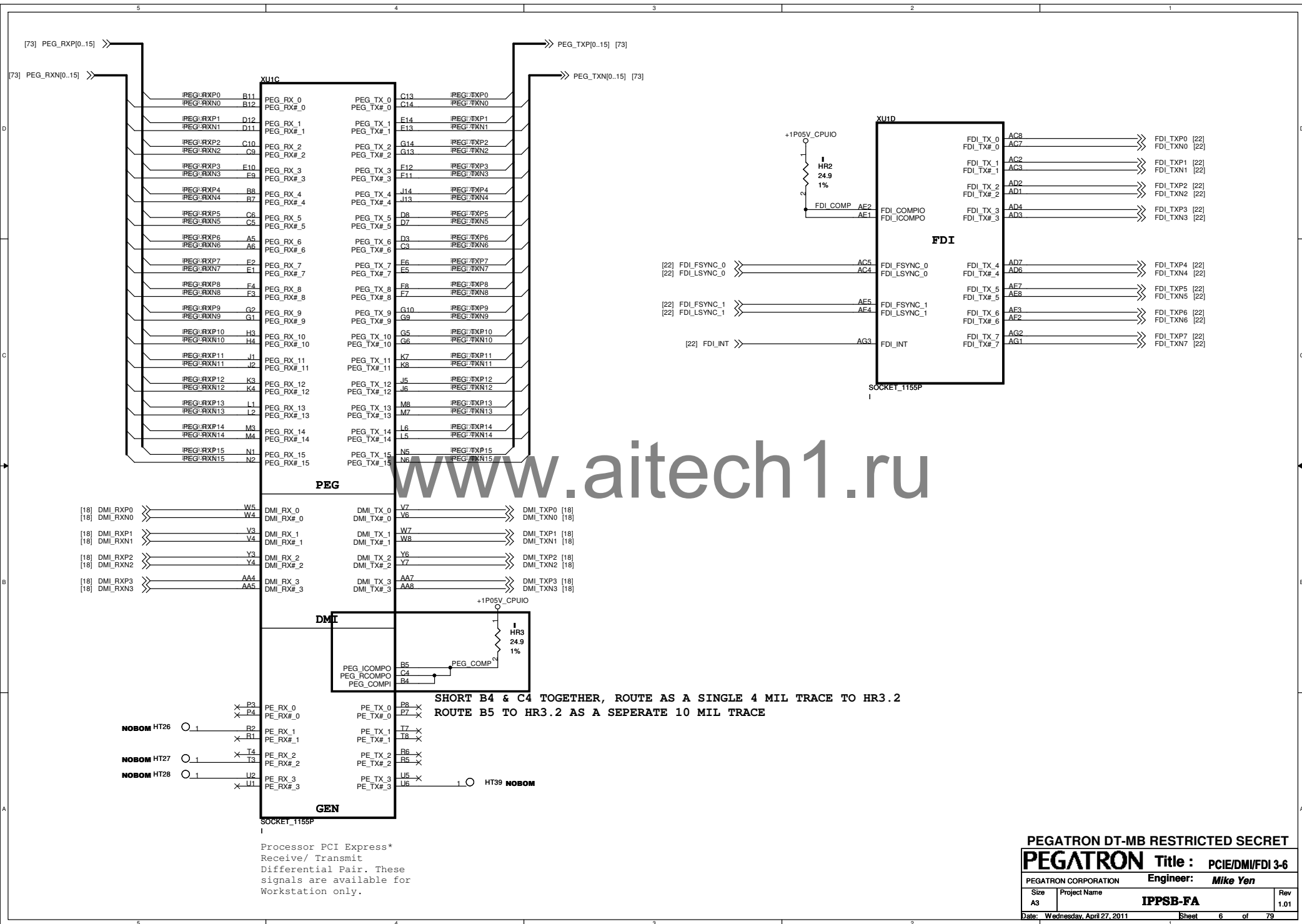


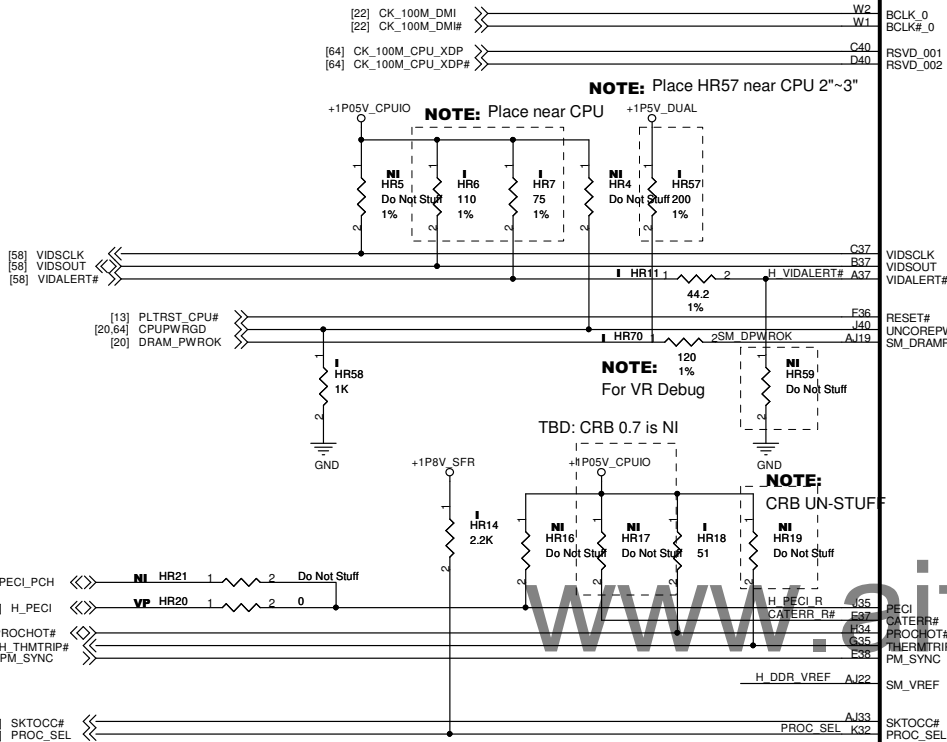




0413

PEGATRON		Title : POWER SEQUENCE	
PEGATRON CORPORATION		Engineer: Mike Yen	
Size	Project Name	Rev	
A3	IPPSB-FA	1.01	
Date: Tuesday, April 26, 2011		Sheet 3 of 79	

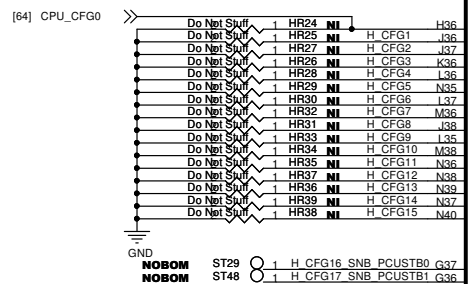
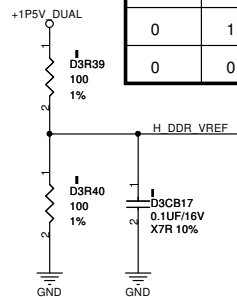


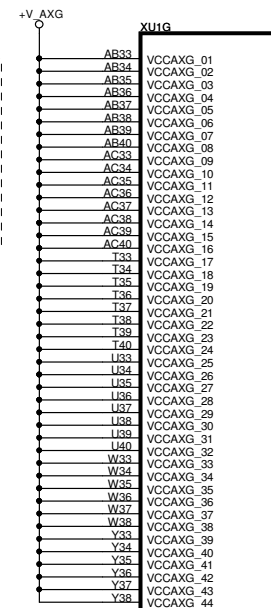
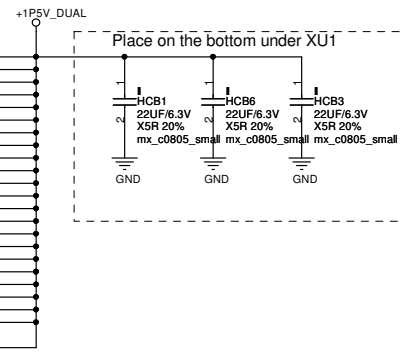
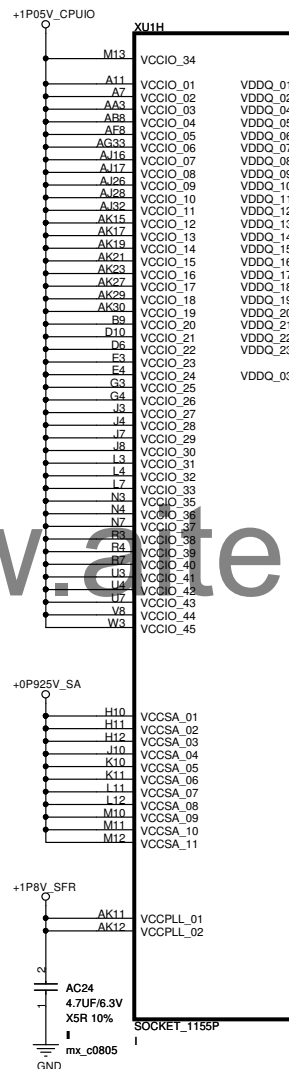
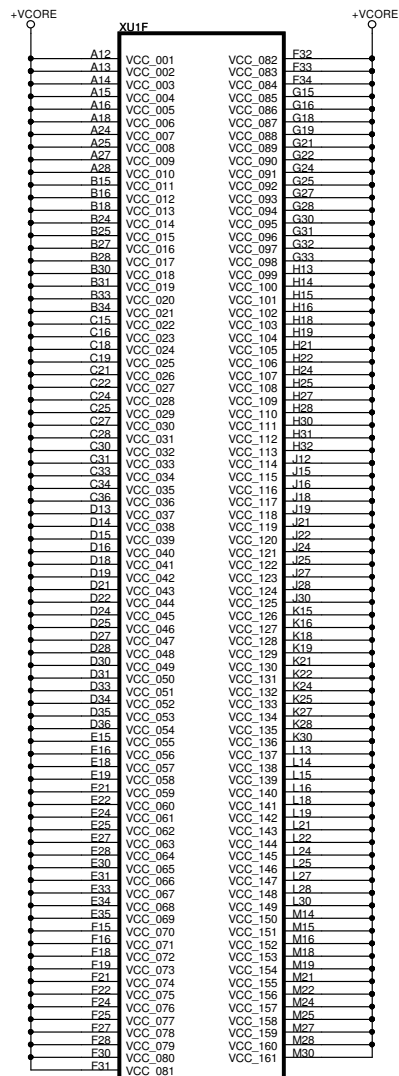


CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
 - 1 = Normal operation
 - 0 = Lane numbers reversed

NOTE: CFG[0~15] is IPU

CFG6	CFG5	Description
1	1	X16(Default)
1	0	2X8
0	1	Reserved
0	0	X8, X4/X4



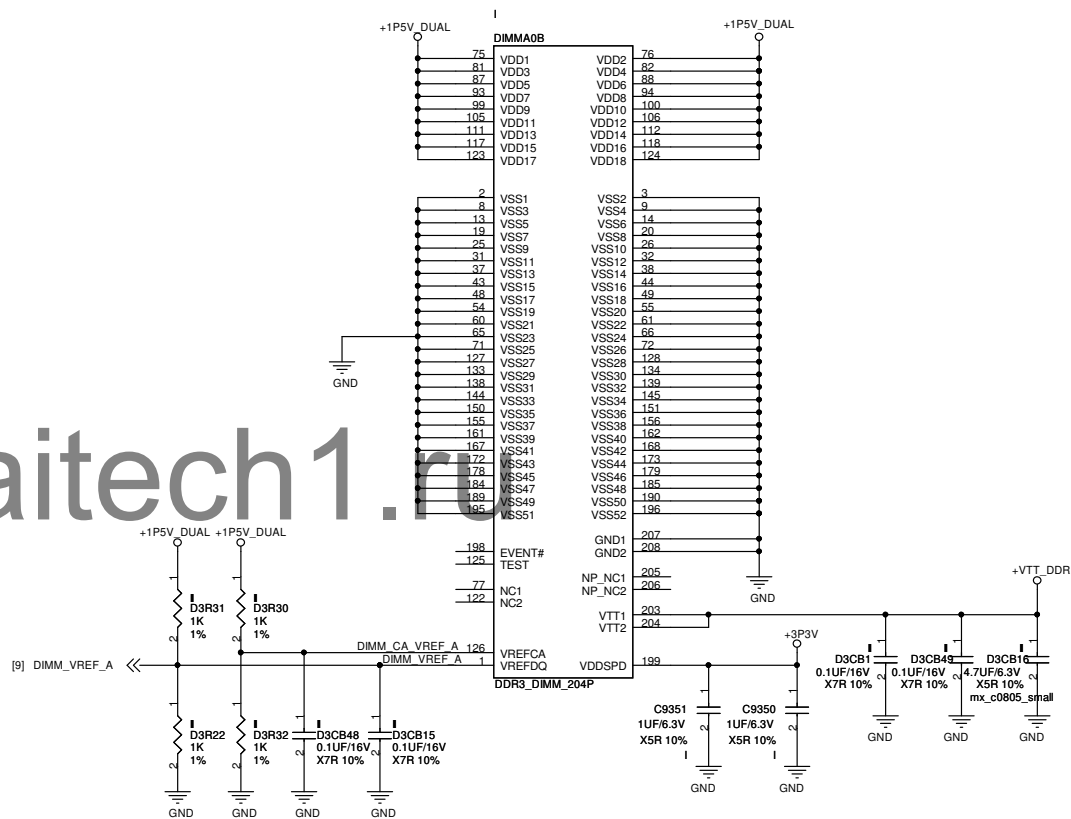
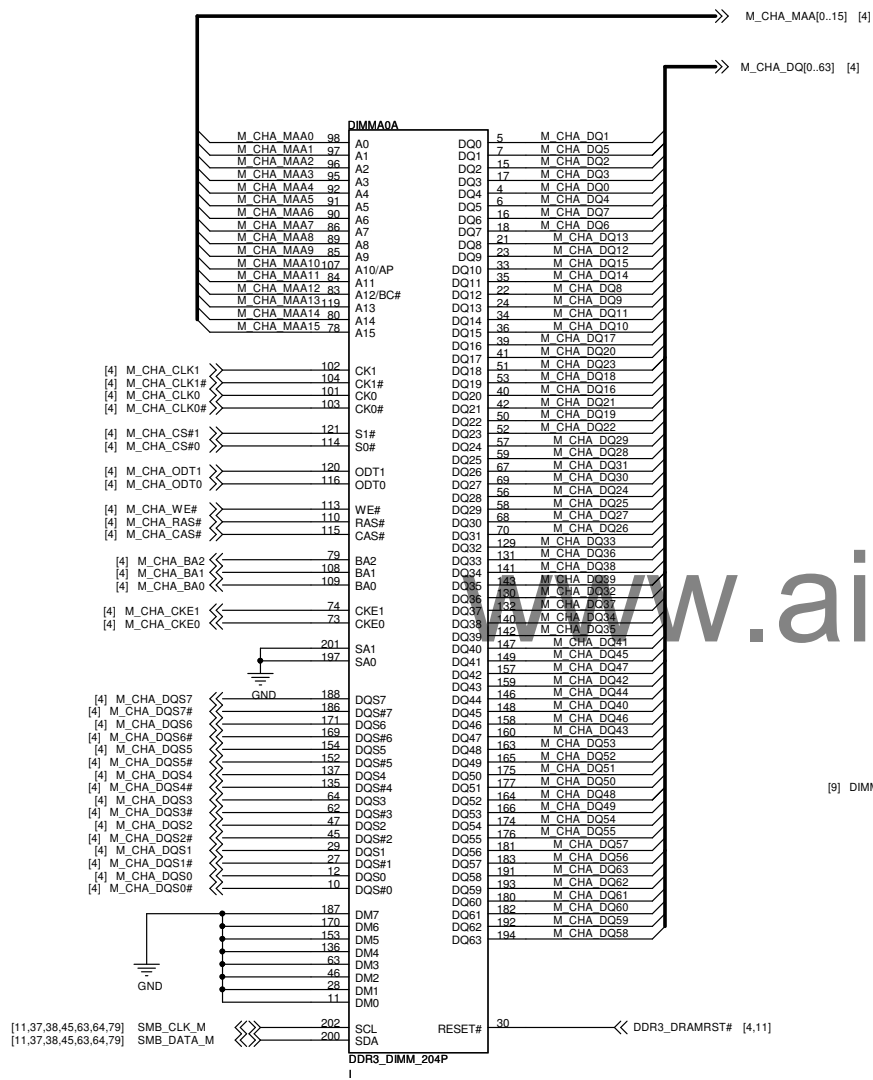


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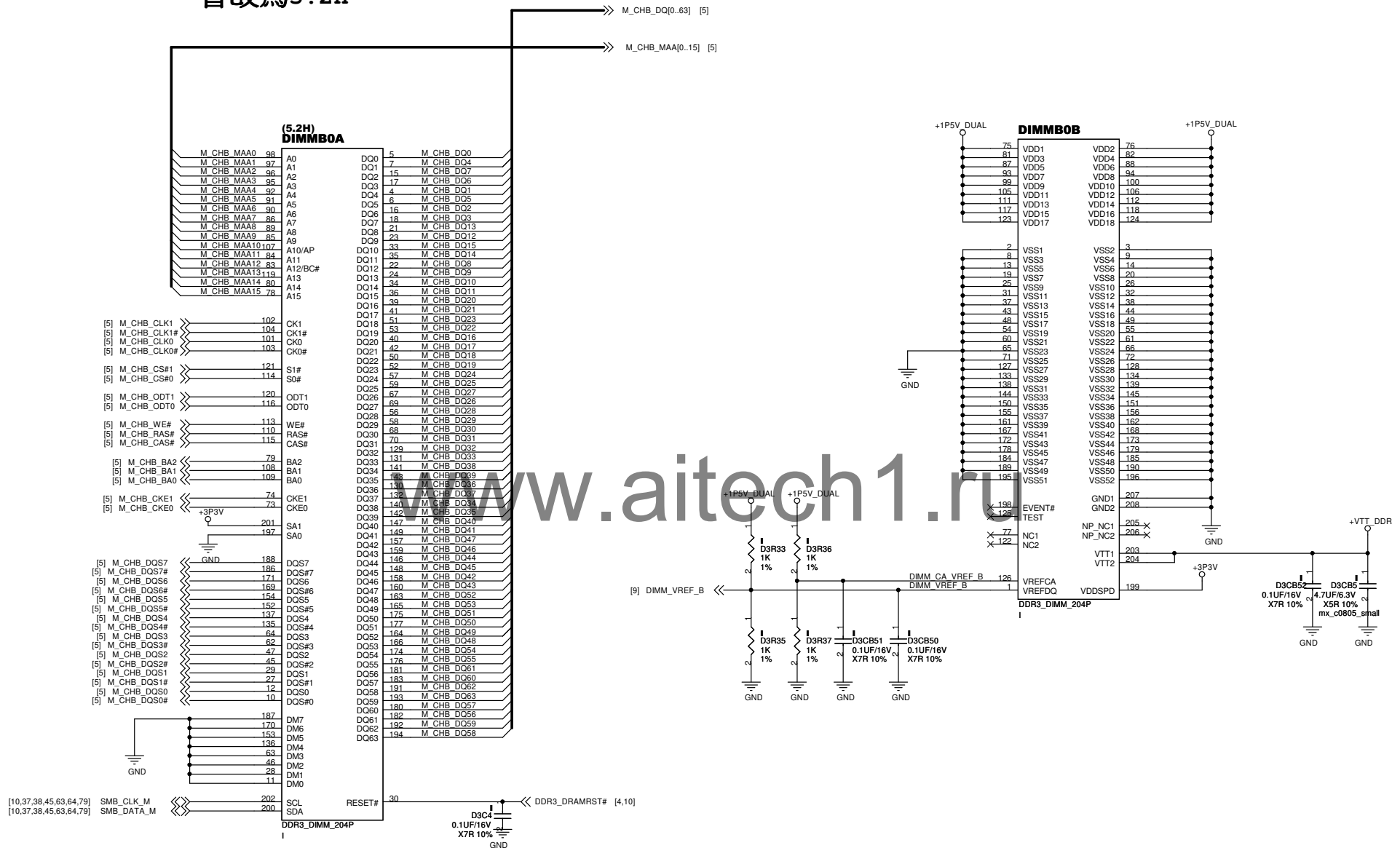
PEGATRON DT-MB RESTRICTED SECRET

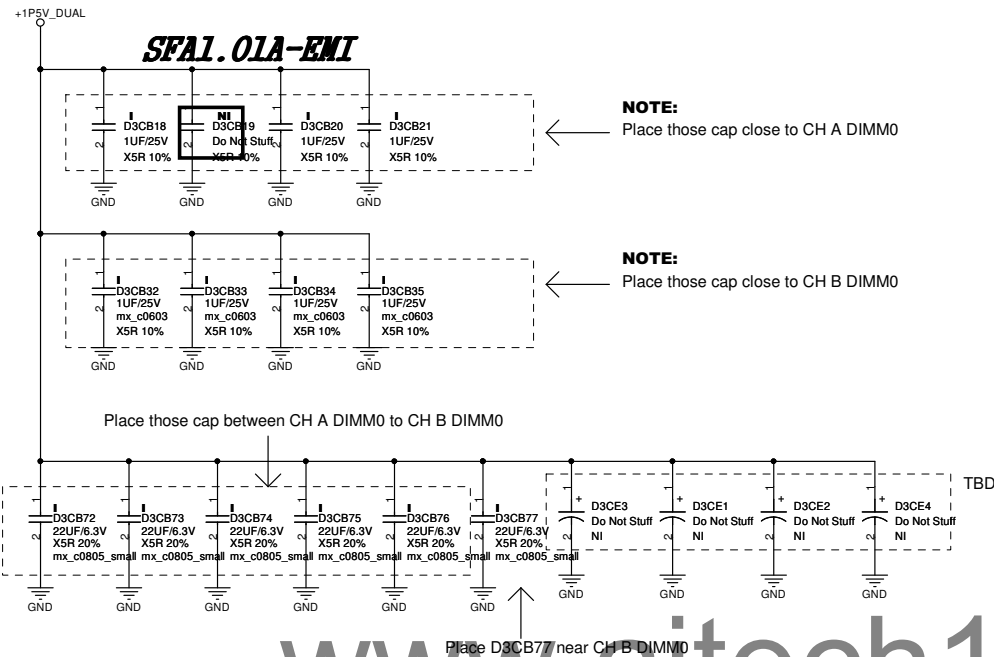
PEGATRON		Title : VCC 5 - 6	
PEGATRON CORPORATION		Engineer: Mike Yen	
Size A3	Project Name IPPSB-FA	Rev 1.01	
Date: Tuesday, April 26, 2011		Sheet 8 of 79	

皆改爲5.2H



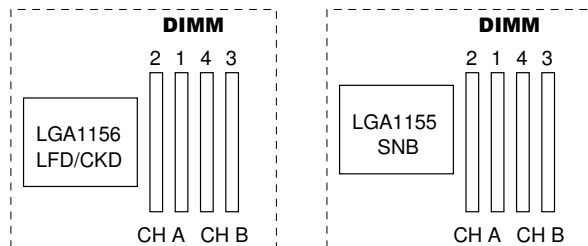
皆改爲5.2H





NOTE:

DIMM Placement for different platform



PEGATRON DT-MB RESTRICTED SECRET

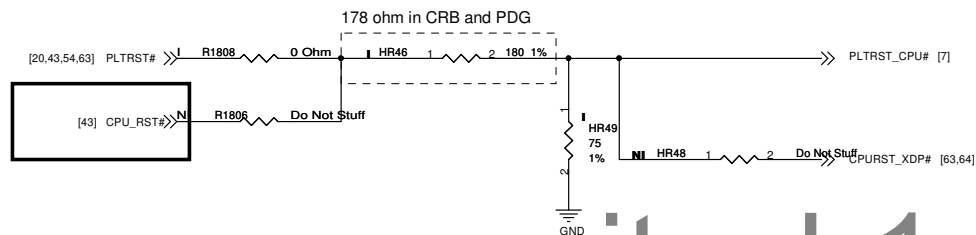
PEGATRON Title : DDR3 TERMINATION A&B

PEGATRON CORPORATION Engineer: Mike Yen

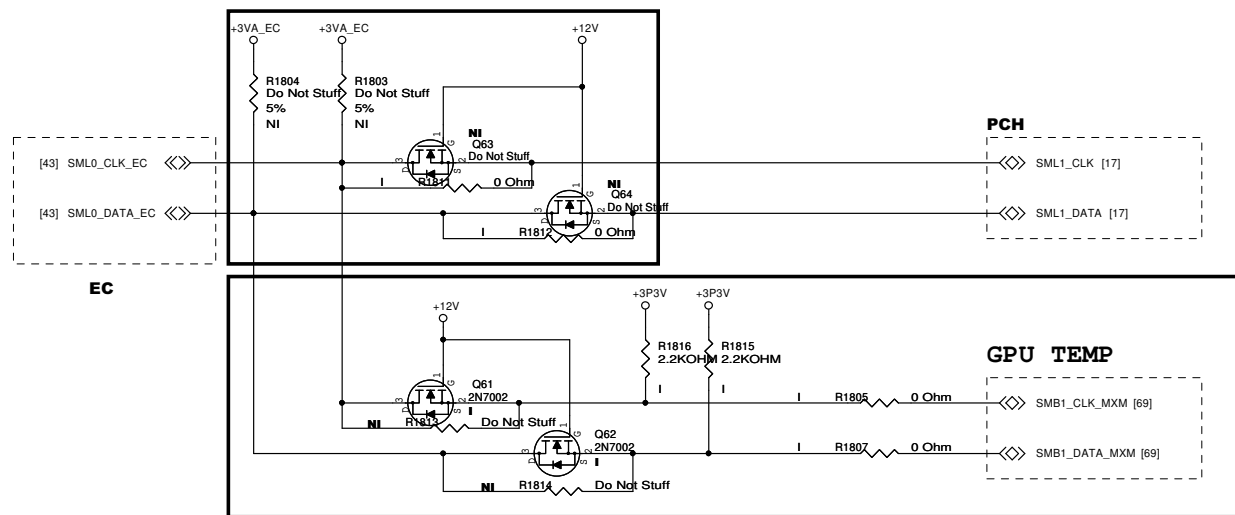
Size A3 Project Name IPPSB-FA Rev 1.01

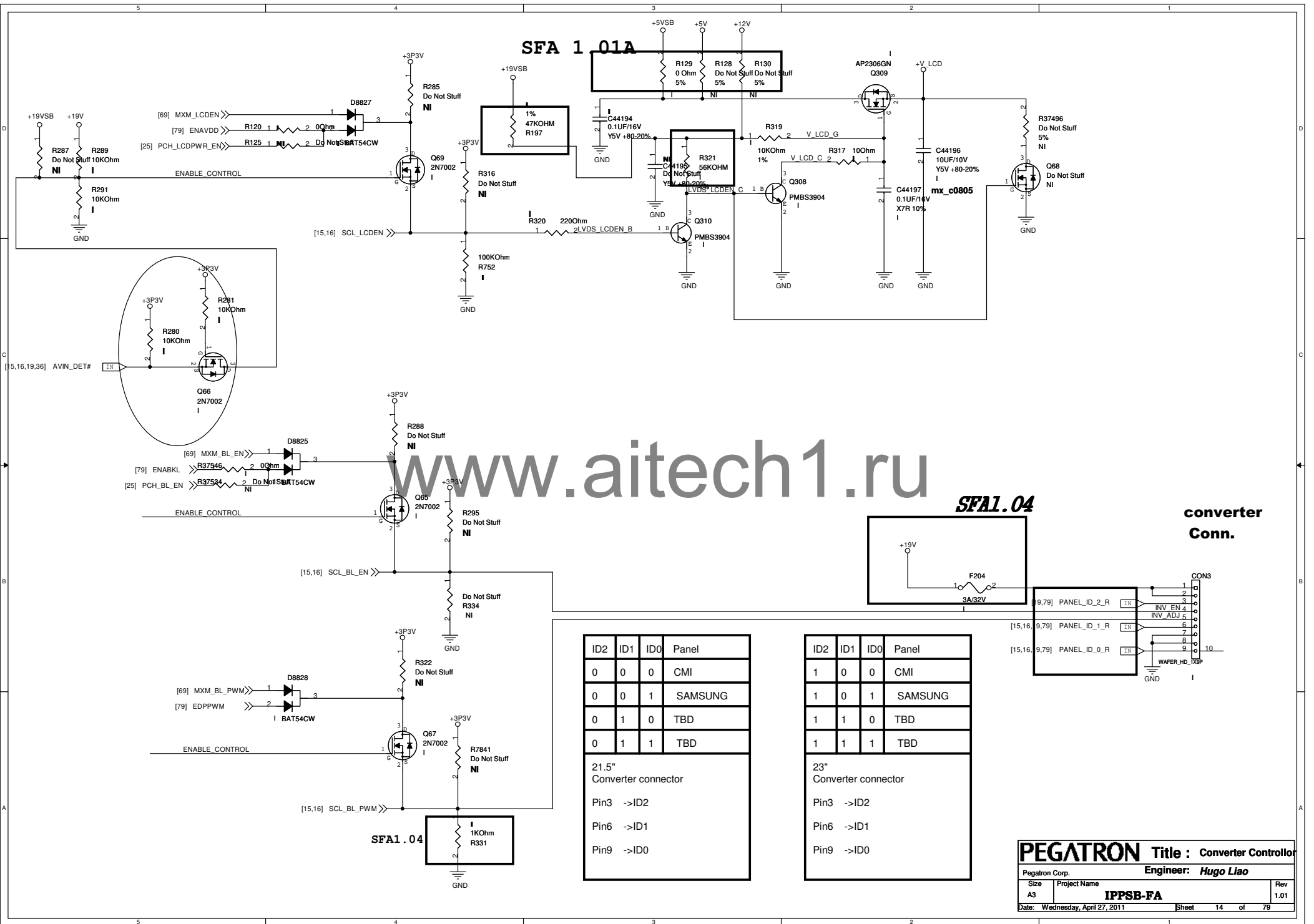
Date: Tuesday, April 26, 2011 Sheet 12 of 79

PLTRST_CPU#

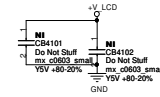
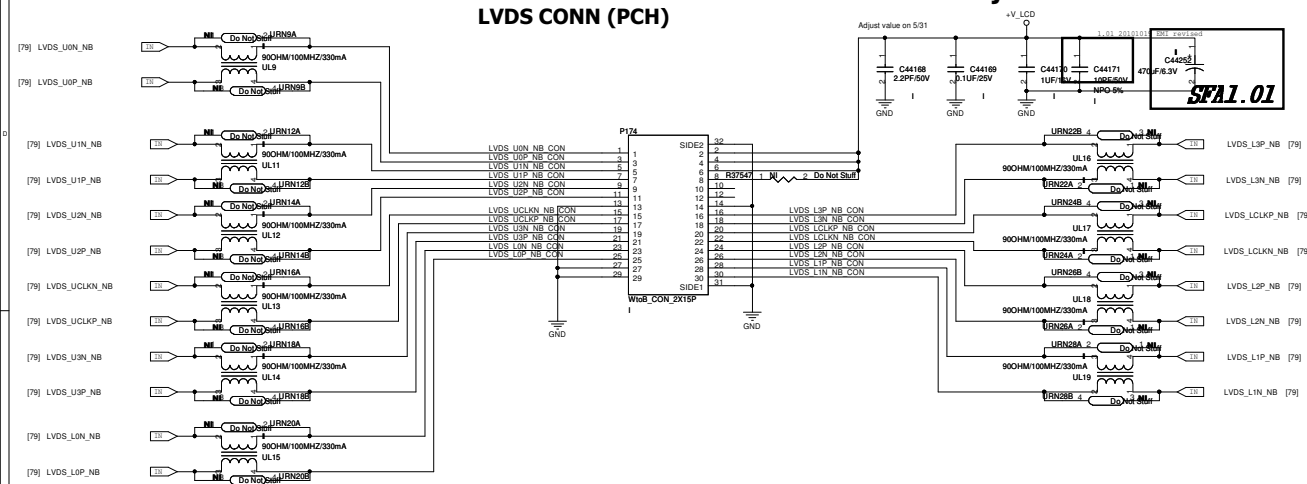


www.aitech1.ru

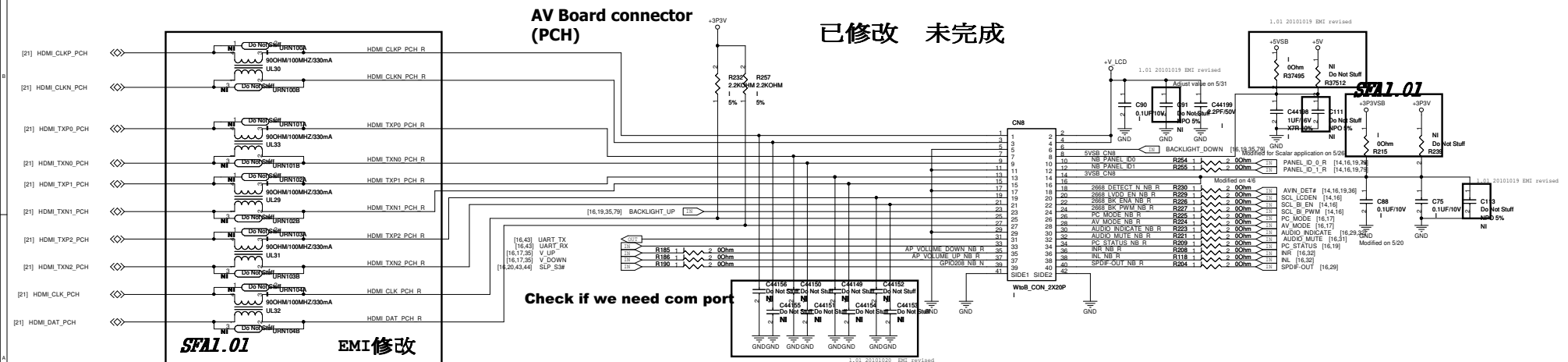




LCD CONN NB & GPU colay



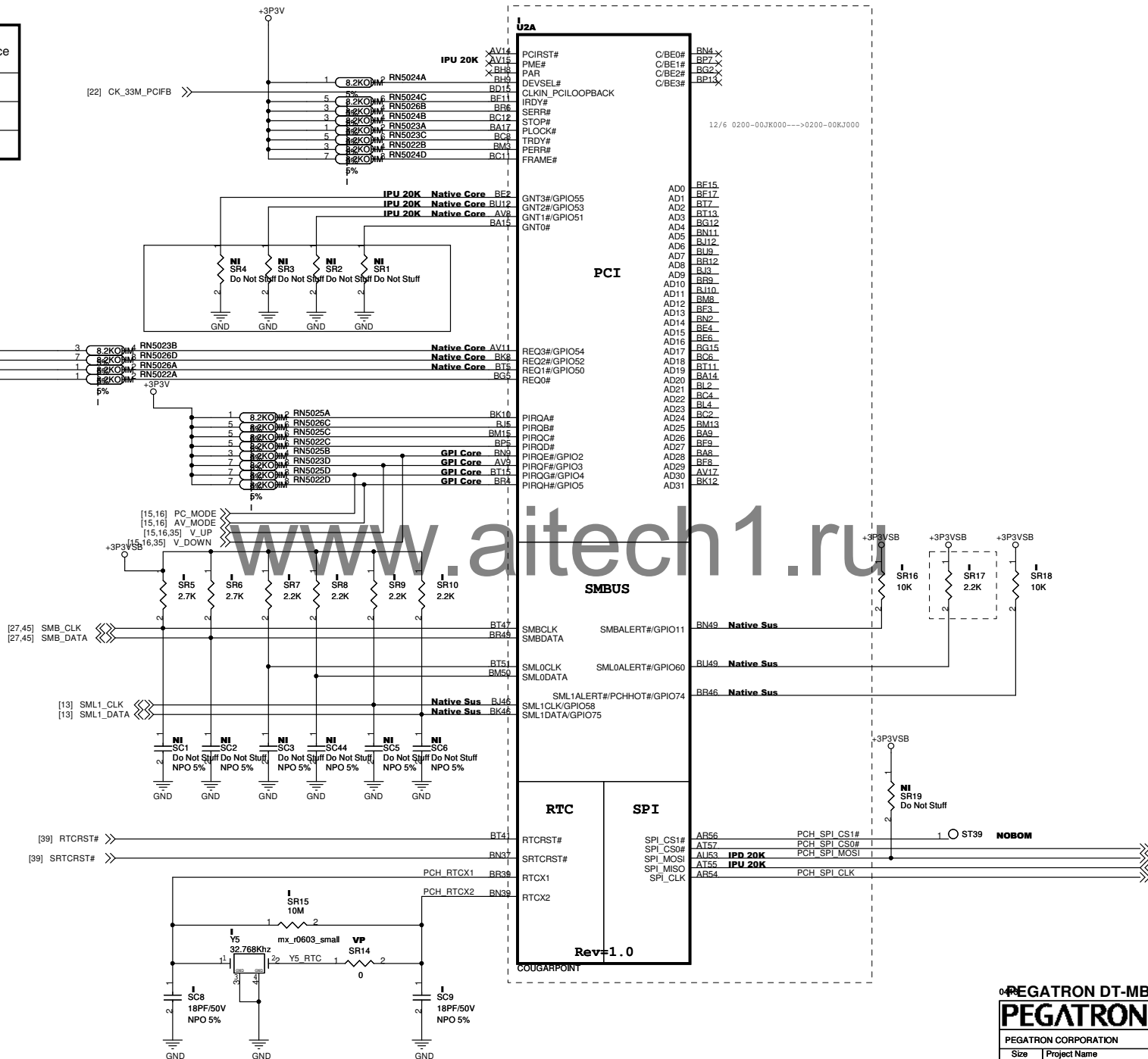
www.aitech1.ru



NOTE: Strapping Options Flash

GNT1#	SATA1GP /GPIO19	Boot Device
0	0	LPC
1	0	PCI
1	1	SPI

I2C/en(dis)able/S3
for accelerometer



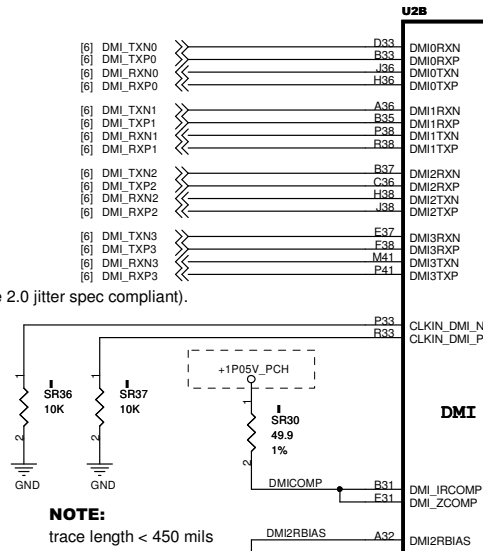
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : PCVSM/SPI/RTC 1-9
PEGATRON CORPORATION		Engineer: Mike Yen
Size A3	Project Name IPPSB-FA	Rev 1.01

Date: Wednesday, April 27, 2011 Sheet 17 of 79

NOTE:

Used for for DMI, PCIe(PCle 2.0 jitter spec compliant).



NOTE:

trace length < 450 mils

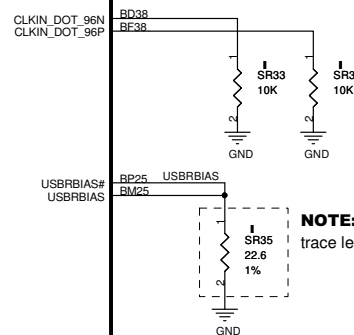
USB

OC0#/GPIO59
OC1#/GPIO40
OC2#/GPIO41
OC3#/GPIO42
OC4#/GPIO43
OC5#/GPIO9
OC6#/GPIO10
OC7#/GPIO14

RM43 Native Sus
RD41 Native Sus
RM41 Native Sus
RM43 Native Sus
BP43 Native Sus
RM41 Native Sus
RM45 Native Sus
RM45 Native Sus
OC01# [35]
OC23# [34]
OC48# [34]
C73C010
R37567D
R37567A
R37567C
R37567B

NOTE:

Used for integrated graphics, generate USB backbone,
24MHz HDA bit, and 48MHz clock.



NOTE:

trace length < 200 mils

side x2 #1 USB Debug port

Rear x4

Touch Panel

CARD READER

#9 USB Debug port

WL

HUB

WLAN

TVT

LAN

for H61,
PCIe ports 7 and 8 are disabled.

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCIe/USB/DMI 2-9

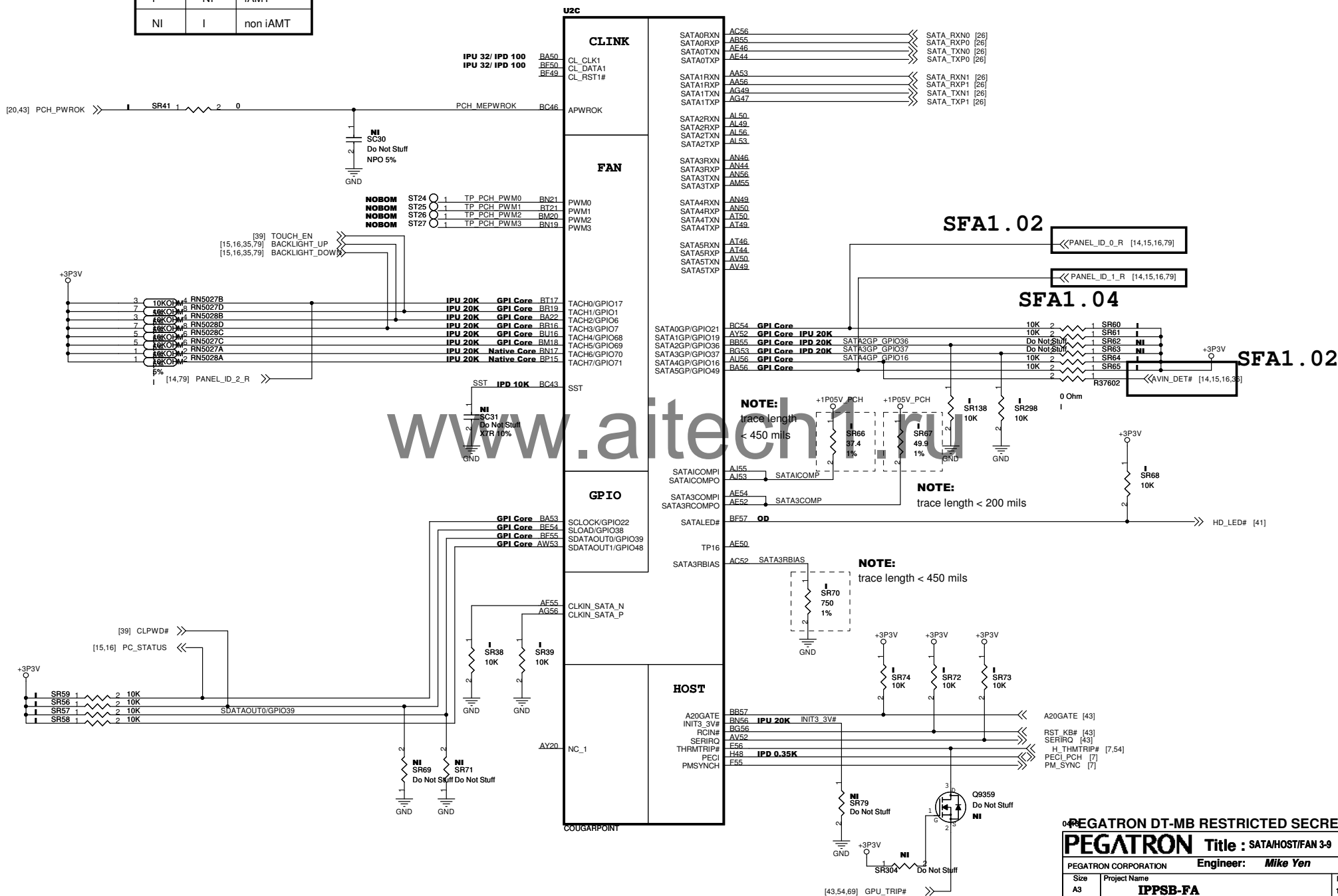
PEGATRON CORPORATION Engineer: Mike Yen

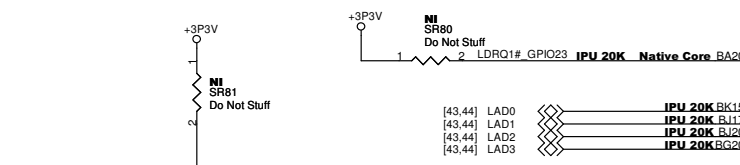
Size Project Name

A3 IPPSB-FA

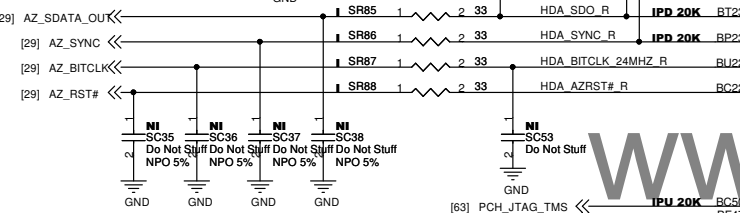
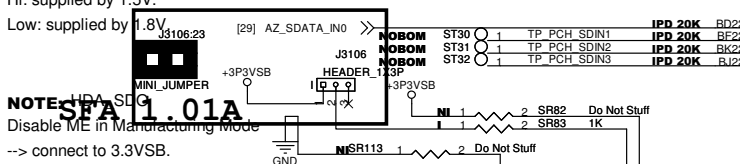
Date: Wednesday, April 27, 2011 Sheet 18 of 79

SR40	SR41	Description
I	NI	iAMT
NI	I	non iAMT

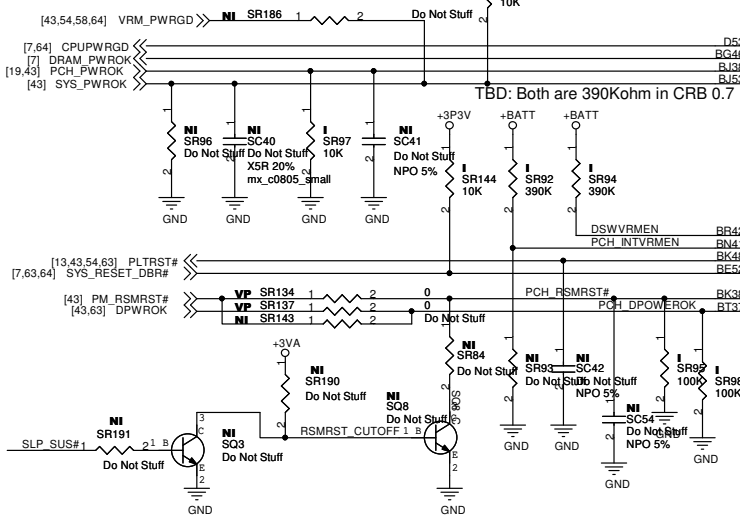




NOTE: HDA_SYNC
On-die PLL VR voltage selector.
Hi: supplied by 1.5V.
Low: supplied by 1.8V.



NOTE: CRB 0.7 is 1.1K ohm with 1%
For platform not supporting deep sleep connect directly to RSMRST#.
The DSW rails must be stable for at least 10 ms before DPWR0K is asserted to PCH.



LPC
LDRQ1#/GPIO23
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
LDRQ0#
FWH4/LFRAME#

AUDIO
HDA_SDO
HDA_SYNC
HDA_BCLK
HDA_RST#

NOTE:
SUSACK# and SUSWARN#
can be tied together if EC/SIO
does not want to involve in
the handshake mechanism
for the Deep Sleep state
entry and exit.

NOTE:
SUSACK# and SUSWARN#
can be tied together if EC/SIO
does not want to involve in
the handshake mechanism
for the Deep Sleep state
entry and exit.

NOTE:
SUSACK# and SUSWARN#
can be tied together if EC/SIO
does not want to involve in
the handshake mechanism
for the Deep Sleep state
entry and exit.

BMBUSY#/GPIO0
CLKRUN#/GPIO32
HDA_DOCK_EN#/GPIO33
STP_PC#/GPIO34
GPIO35
GPIO36
LAN_PHY_PWR_CTRL#/GPIO12
HDA_DOCK_RST#/GPIO13
GPIO15
GPIO24/MEM_LED
GPIO28
SLP_LAN#/GPIO29
GPIO27
GPIO31

BATLOW#/GPIO72
SUSWARN#/SUSPWRDNACK#/GPIO30
SUSACK#
SUSCLK#/GPIO62
SUS_STAT#/GPIO61

SLP_S3#
SLP_S4#
SLP_S5#/GPIO63
SLP_A#
SLP_SUS#

SLP_S3#
SLP_S4#
SLP_S5#/GPIO63
SLP_A#
SLP_SUS#

AW55 **GPI Core**
BC56 **GPO Core** CLKRUN# GPIO32
BC25 **GPO Core** HDA_DOCK_EN# GPIO33
BL56 **GPI Core** STP_PC# GPIO34
BJ57 **GPI Core**
BP51 **GPO Sus** **IPU 20K**
BK50 **Native Sus**
BA25 **GPI Sus**
BM55 **GPO Sus** **IPD 20K**
BC53 **GPO Sus** GPIO24 MEM_LED
BJ55 **GPO Sus** **IPU 20K**
BH49 **GPI Sus**
BJ43 **GPI DSW** **IPU 20K**
BG43 **GPI DSW** **IPD T8D**

AV45 **Native Sus** **IPU 20K**
BJ45 **Native Sus** **IPU T8D**
AV44 **Native Sus** **IPU 20K**
BP55 **Native Sus** **IPU 20K**
BT53 **GPI Sus**

RI#
WAKE#
INTRUDER#
SPKR
PWRBTN#

BM53
BN52
BH59 **Native Sus**
BD41
BD43 **O**

AW55 **GPI Core**
BC56 **GPO Core** CLKRUN# GPIO32
BC25 **GPO Core** HDA_DOCK_EN# GPIO33
BL56 **GPI Core** STP_PC# GPIO34
BJ57 **GPI Core**
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BJ55 **GPO Sus** **IPU 20K**
BH49 **GPI Sus**
BJ43 **GPI DSW** **IPU 20K**
BG43 **GPI DSW** **IPD T8D**

AV45 **Native Sus** **IPU 20K**
BJ45 **Native Sus** **IPU T8D**
AV44 **Native Sus** **IPU 20K**
BP55 **Native Sus** **IPU 20K**
BT53 **GPI Sus**

RI#
WAKE#
INTRUDER#
SPKR
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BM53
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BC56 **GPO Core** CLKRUN# GPIO32
BC25 **GPO Core** HDA_DOCK_EN# GPIO33
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BJ55 **GPO Sus** **IPU 20K**
BH49 **GPI Sus**
BJ43 **GPI DSW** **IPU 20K**
BG43 **GPI DSW** **IPD T8D**

AV45 **Native Sus** **IPU 20K**
BJ45 **Native Sus** **IPU T8D**
AV44 **Native Sus** **IPU 20K**
BP55 **Native Sus** **IPU 20K**
BT53 **GPI Sus**

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AW55 **GPI Core**
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BC25 **GPO Core** HDA_DOCK_EN# GPIO33
BL56 **GPI Core** STP_PC# GPIO34
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BM55 **GPO Sus** **IPD 20K**
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BJ55 **GPO Sus** **IPU 20K**
BH49 **GPI Sus**
BJ43 **GPI DSW** **IPU 20K**
BG43 **GPI DSW** **IPD T8D**

AV45 **Native Sus** **IPU 20K**
BJ45 **Native Sus** **IPU T8D**
AV44 **Native Sus** **IPU 20K**
BP55 **Native Sus** **IPU 20K**
BT53 **GPI Sus**

RI#
WAKE#
INTRUDER#
SPKR
PWRBTN#

BM53
BN52
BH59 **Native Sus**
BD41
BD43 **O**

AW55 **GPI Core**
BC56 **GPO Core** CLKRUN# GPIO32
BC25 **GPO Core** HDA_DOCK_EN# GPIO33
BL56 **GPI Core** STP_PC# GPIO34
BJ57 **GPI Core**
BP51 **GPO Sus** **IPU 20K**
BK50 **Native Sus**
BA25 **GPI Sus**
BM55 **GPO Sus** **IPD 20K**
BC53 **GPO Sus** GPIO24 MEM_LED
BJ55 **GPO Sus** **IPU 20K**
BH49 **GPI Sus**
BJ43 **GPI DSW** **IPU 20K**
BG43 **GPI DSW** **IPD T8D**

AV45 **Native Sus** **IPU 20K**
BJ45 **Native Sus** **IPU T8D**
AV44 **Native Sus** **IPU 20K**
BP55 **Native Sus** **IPU 20K**
BT53 **GPI Sus**

RI#
WAKE#
INTRUDER#
SPKR
PWRBTN#

BM53
BN52
BH59 **Native Sus**
BD41
BD43 **O**

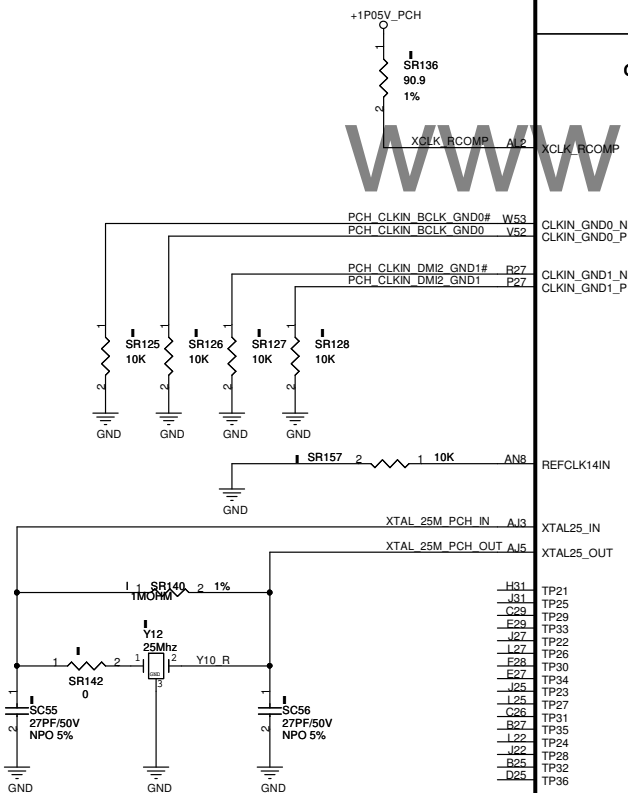
NOTE:
PDG 0.7 is 1Kohm

NOTE:
GPIO27 can be configured as wake input
to allow wakes from Deep Sleep.
NOTE:
External PU resistor required
if used for CLKREQ# functionality.

PIN	HIGH	LOW	DESCRIPTION
GPIO15	Enable	Disable	TLS confidentiality
GPIO28	Enable	Disable	On-Die PLL VR

[7] PROC_SEL

Place HR23 close to NVRAM connector
and minimize this stub to <100 mils
with PCH and NVRAM connector



U2F

FDI

RSD

CLOCK

FDI_RXN0
FDI_RXP0
FDI_RXN1
FDI_RXP1
FDI_RXN2
FDI_RXP2
FDI_RXN3
FDI_RXP3
FDI_RXN4
FDI_RXP4
FDI_RXN5
FDI_RXP5
FDI_RXN6
FDI_RXP6
FDI_RXN7
FDI_RXP7

FDI_FSYNCO
FDI_LSYNCO
FDI_FSYNC1
FDI_LSYNC1
FDI_INT

FDI_FSYNC0 [6]
FDI_LSYNC0 [6]
FDI_FSYNC1 [6]
FDI_LSYNC1 [6]
FDI_INT [6]

Reserved_001
Reserved_002
Reserved_003
Reserved_004
Reserved_005
Reserved_006
Reserved_007
Reserved_008
Reserved_009
Reserved_010
Reserved_011
Reserved_012
Reserved_013
Reserved_014
Reserved_015
Reserved_016
Reserved_017
Reserved_018
Reserved_019
Reserved_020
Reserved_021
Reserved_022
Reserved_023
Reserved_024
Reserved_025
Reserved_026
Reserved_027
Reserved_028
Reserved_029

AB50
Y50
AB49
AB44
L449
B44
L450
L446
L44
H50
K46
L56
J55
F53
H52
F52
R50 TP_NV_RCOMP 1 ST1 NOBOM

CLKOUT_ITPXD_P_N
CLKOUT_ITPXD_P_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKOUT_PCIE7N
CLKOUT_PCIE7P
CLKOUT_PCIE6N
CLKOUT_PCIE6P
CLKOUT_PCIE5N
CLKOUT_PCIE5P
CLKOUT_PCIE4N
CLKOUT_PCIE4P
CLKOUT_PCIE3N
CLKOUT_PCIE3P
CLKOUT_PCIE2N
CLKOUT_PCIE2P
CLKOUT_PCIE1N
CLKOUT_PCIE1P
CLKOUT_PCIE0N
CLKOUT_PCIE0P
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
CLKOUT_PCIO
CLKOUT_PC1
CLKOUT_PC2
CLKOUT_PC3
CLKOUT_PC4
CLKOUT_FLEX0/GPIO64
CLKOUT_FLEX1/GPIO65
CLKOUT_FLEX2/GPIO66
CLKOUT_FLEX3/GPIO67

SR147 1 2 0
SR148 1 2 0
SR229 1 2 0
SR230 1 2 0
SR231 1 2 0
SR232 1 2 0
SR233 1 2 0
SR234 1 2 0
SR241 1 2 0
SR242 1 2 0
SR235 1 2 0
SR236 1 2 0
SR239 1 2 0
SR240 1 2 0
SR262 1 2 22 OHM
SR251 1 2 22 OHM
SR253 1 2 22 OHM
SR264 1 2 22 OHM
SR265 1 2 22 OHM
SR266 1 2 22 OHM

CK_100M_CPUXDP# [64]
CK_100M_CPUXDP [64]
CK_100M_DMI# [7]
CK_100M_DMI [7]
CLK_100M_MINI4# [38]
CLK_100M_MINI4 [38]
CLK_100M_MINI1# [37]
CLK_100M_MINI1 [37]
CK_100M_PCHXDP# [63]
CK_100M_PCHXDP [63]
CK_100M_LAN# [27]
CK_100M_LAN [27]
CLK_PEGA# [73]
CLK_PEGA [73]
CLK_DBGPC1 [44]
CLK_KBCPC1 [43]
CK_33M_PCIFB [17]
CK_27M_eDP [79]
CK_48M_CR [78]
CK_27M_GPU [69]

SFA1.01

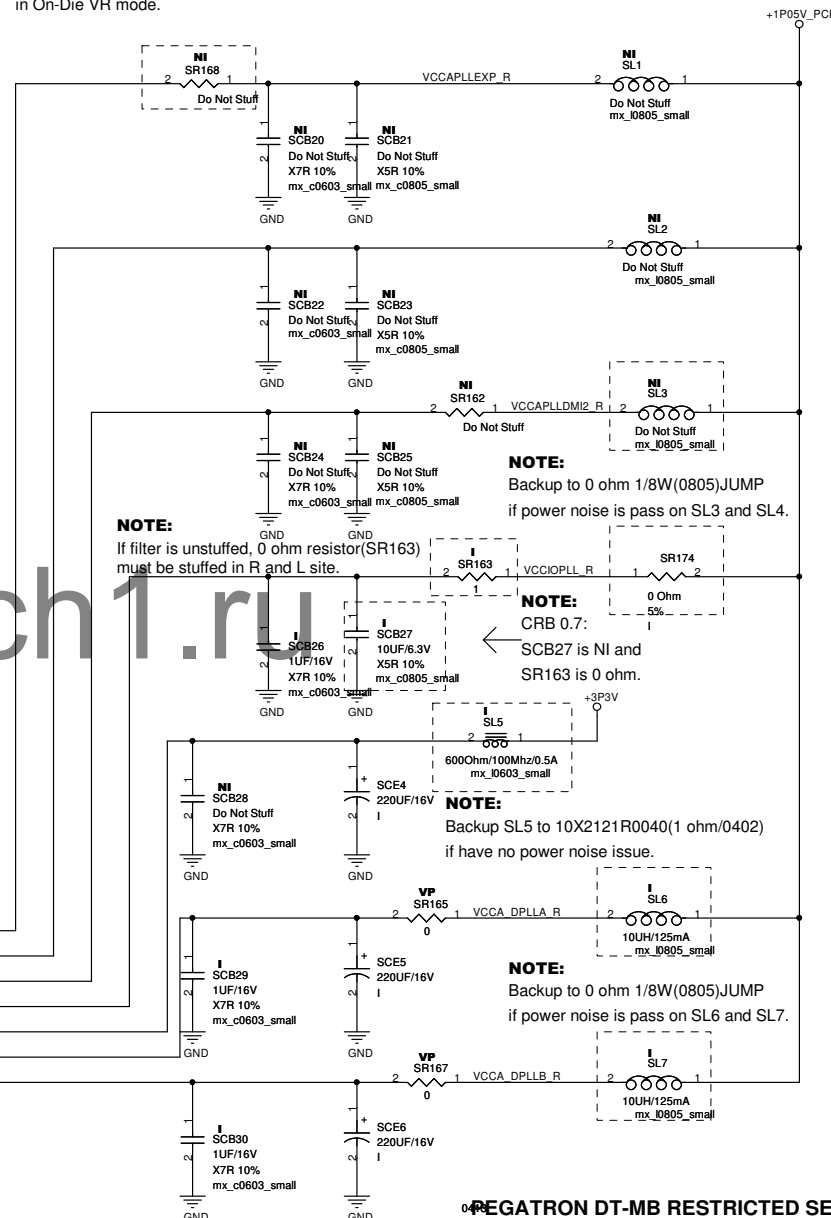
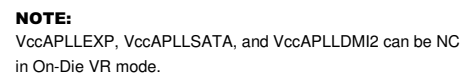
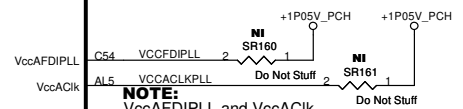
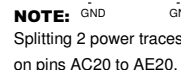
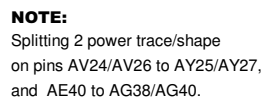
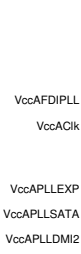
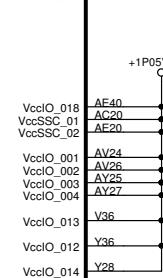
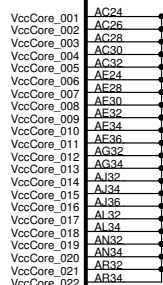
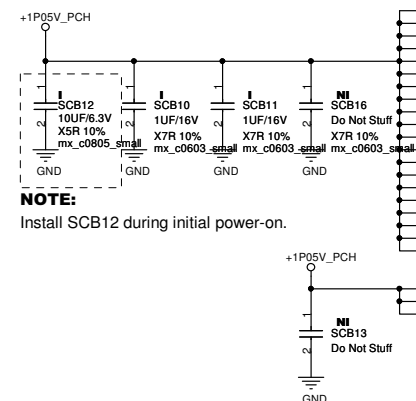
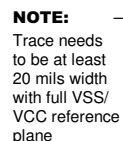
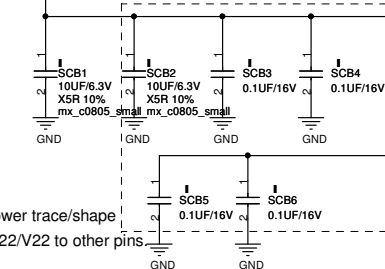
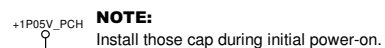
NOTE:

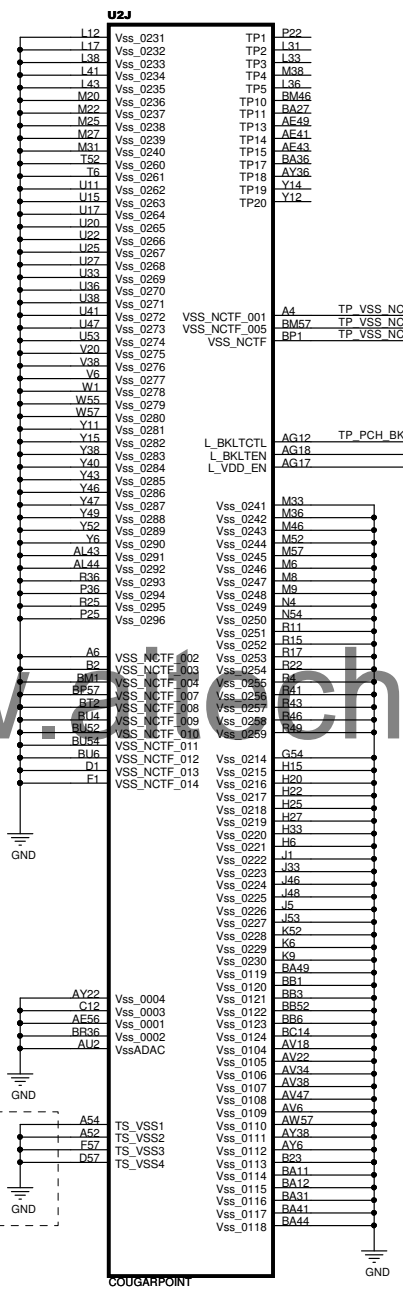
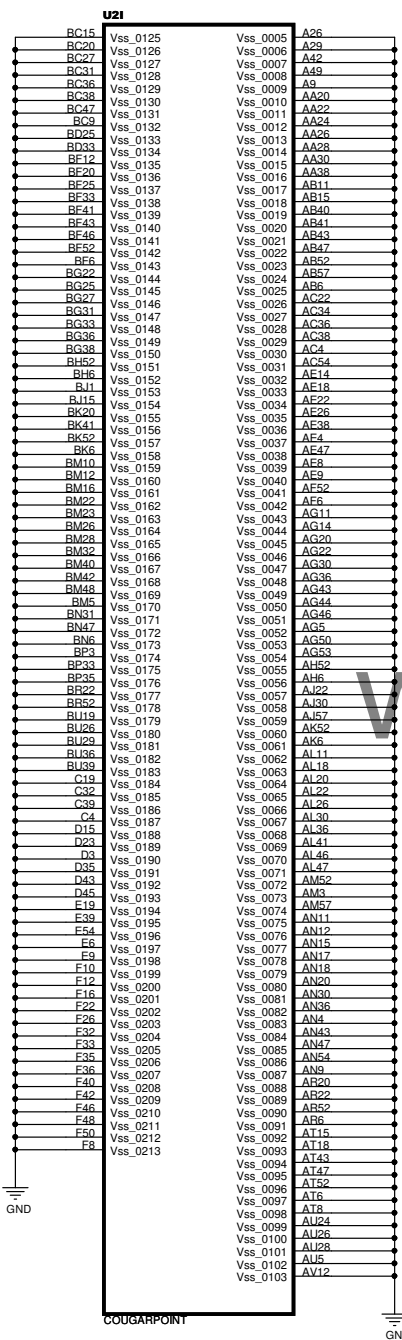
1. Prioritize 27/14/24/48/25-MHz FLEX on FLEX1/3.
2. Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0/2 if more than 2 PCI clocks + PCI loopback are routed.
3. With 2 PCI clocks routed (or less), prioritize the FLEX clocks to FLEX1/3 a. 27MHz(SSC/non-SSC) b. 14.31818MHz c. 24/48 d. 25MHz

PEGATRON DT-MB RESTRICTED SECRET
0413

PEGATRON Title : CLK/NVRAM/FDI 6-9
PEGATRON CORPORATION Engineer: Mike Yen

Size	Project Name	Rev
A3	IPPSB-FA	1.01
Date:	Wednesday, April 27, 2011	Sheet 22 of 79



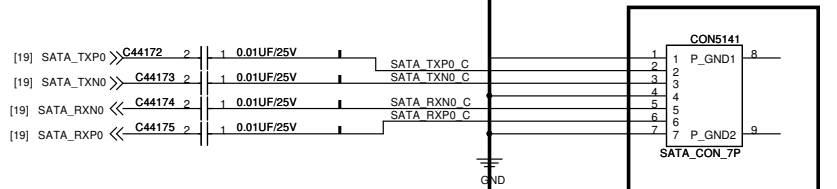


NOTE:
BOM option depend on thermal result

已更改完成

SATA HDD CON

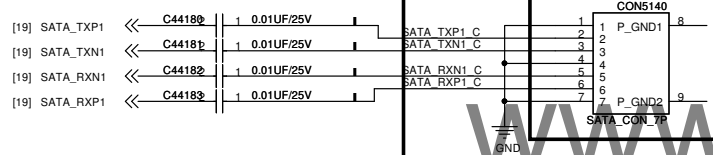
1.01 20101019 revised



**SATA CONTROLLER #1
(MASTER)
COLOR = DARK BLUE**

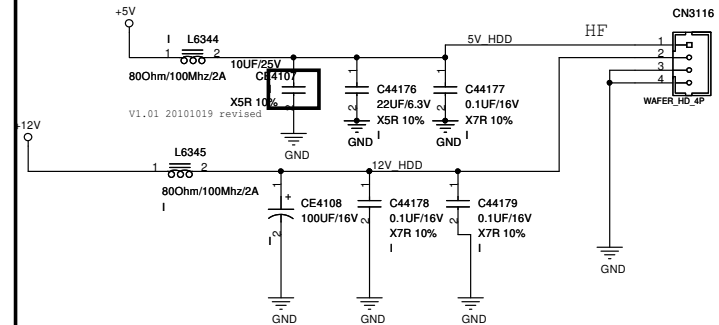
SATA ODD CON

1.01 20101019 revised

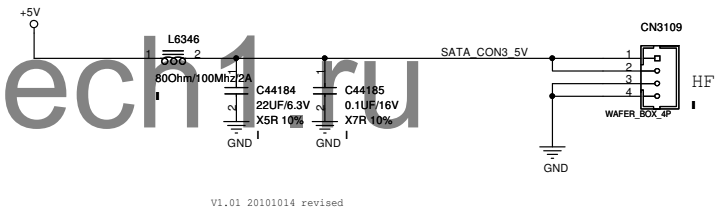


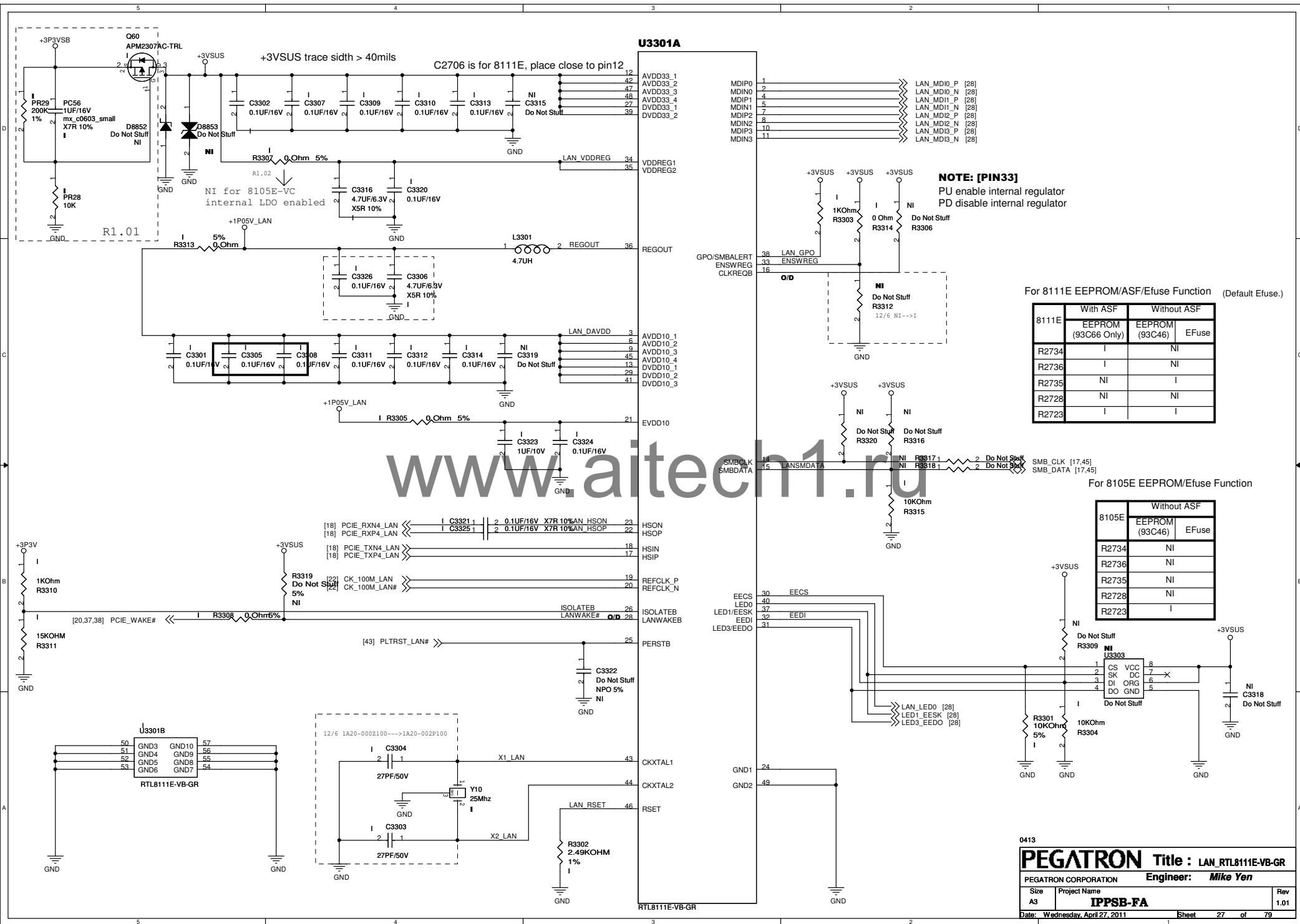
**SATA CONTROLLER #2
(SLAVE)
COLOR = WHITE**

SATA POWER CONN.

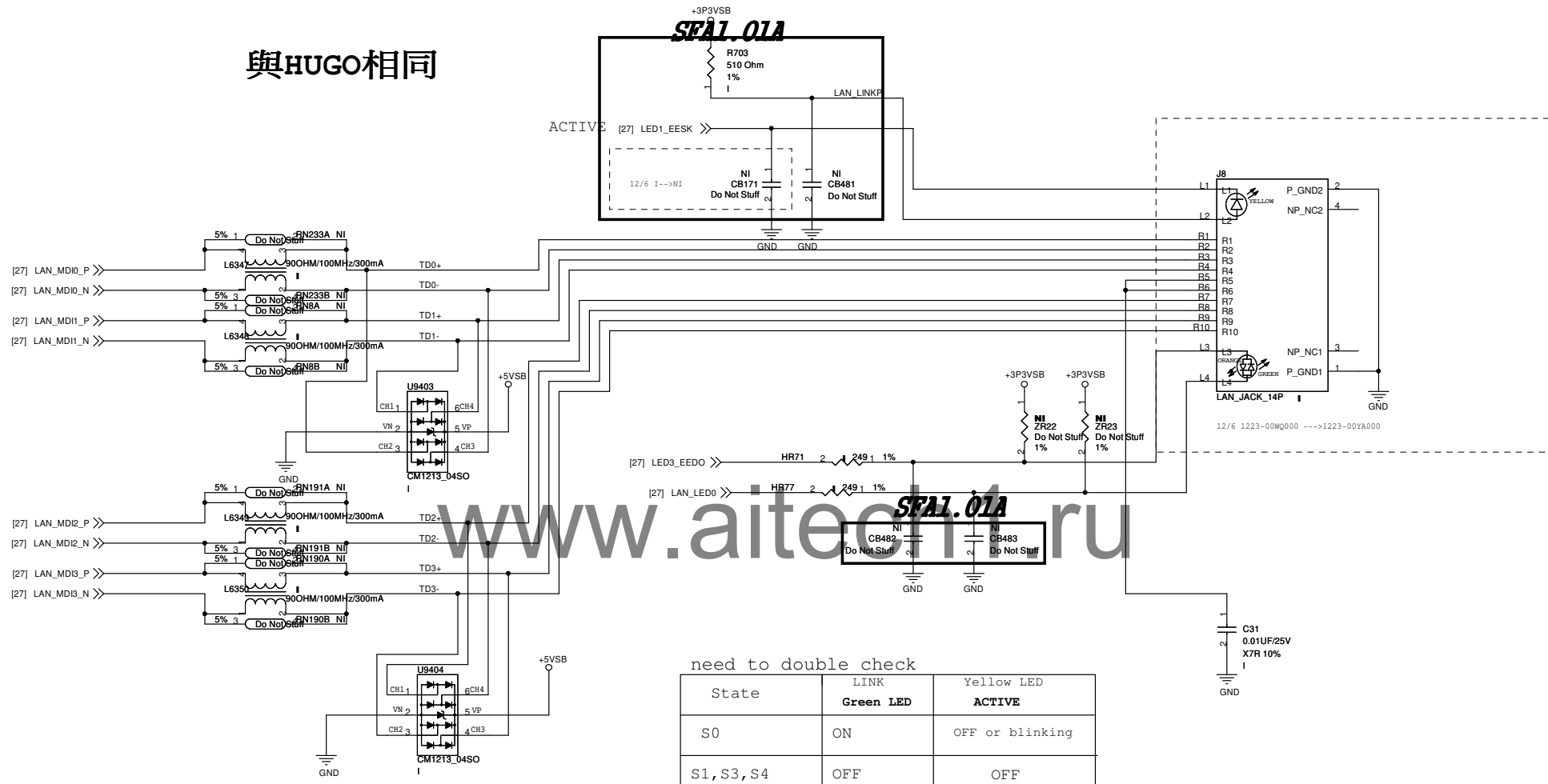


ODD POWER CONN.



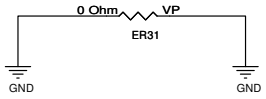


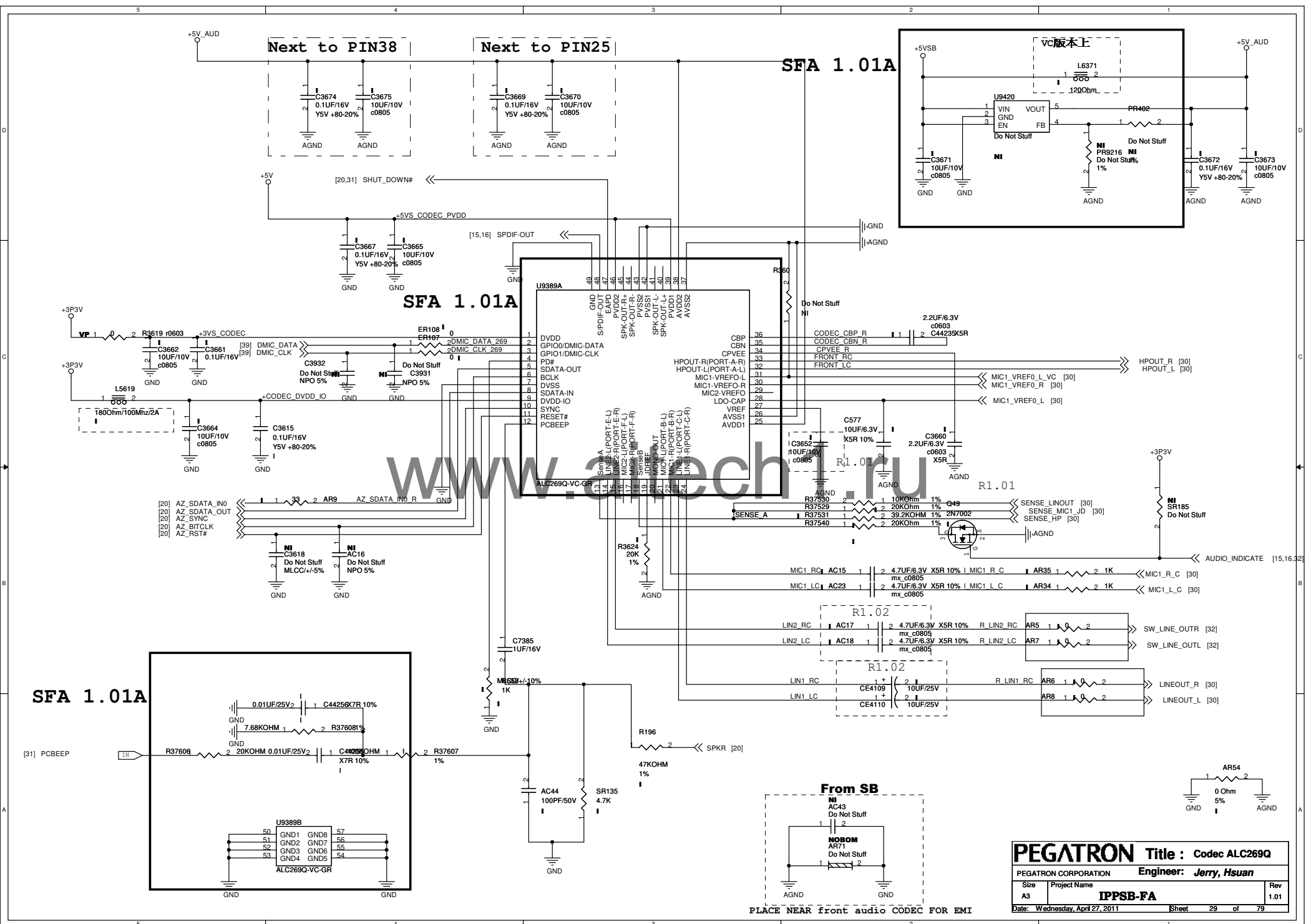
與HUGO相同

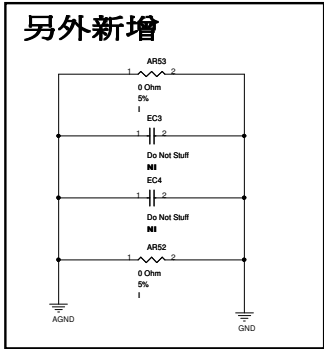
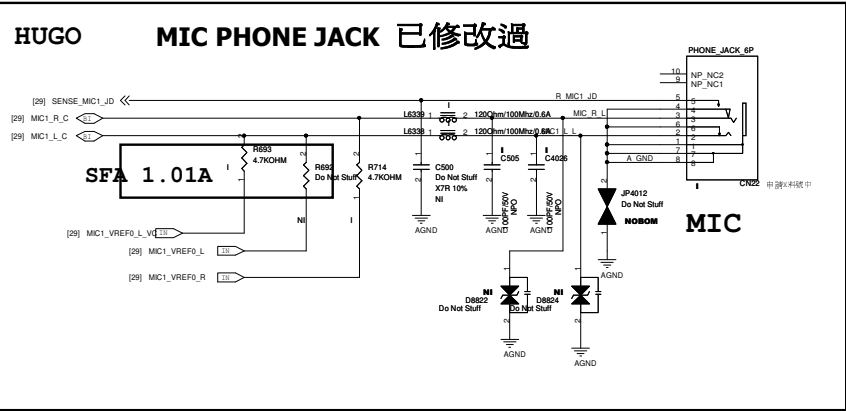
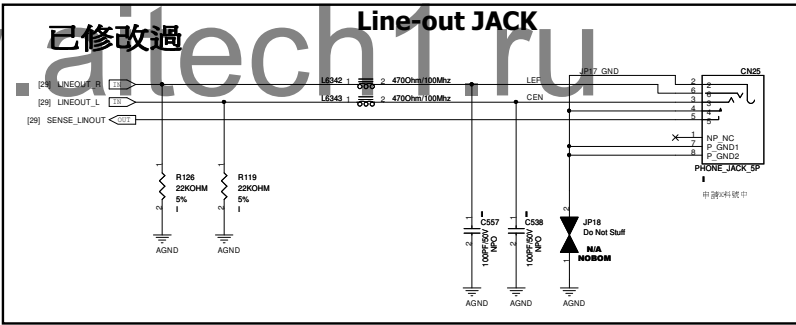
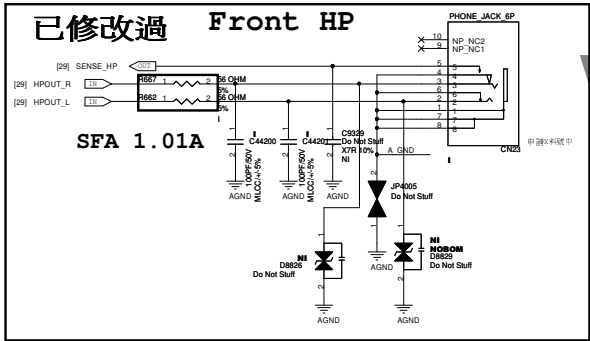


need to double check

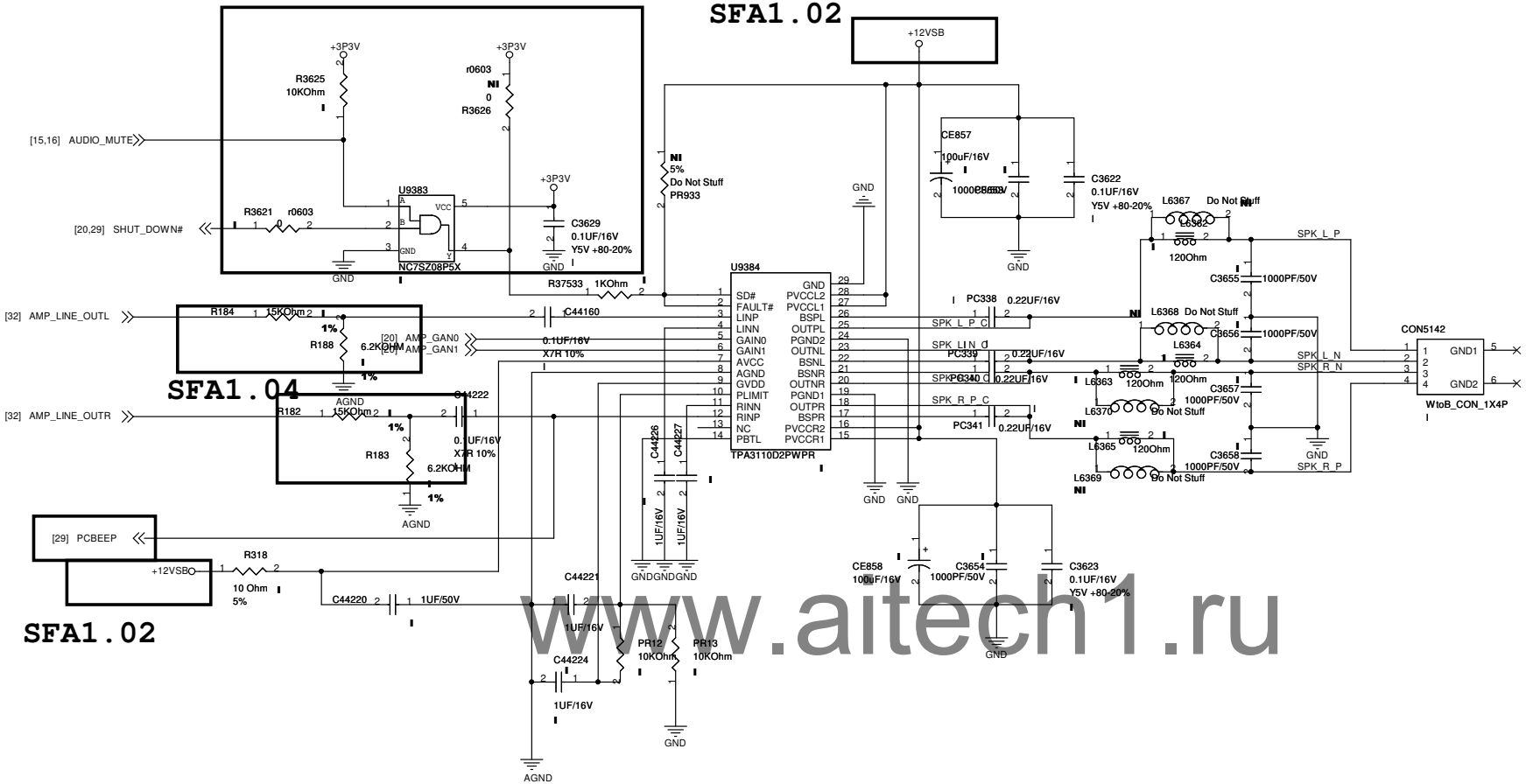
State	LINK Green LED	Yellow LED ACTIVE
S0	ON	OFF or blinking
S1, S3, S4	OFF	OFF





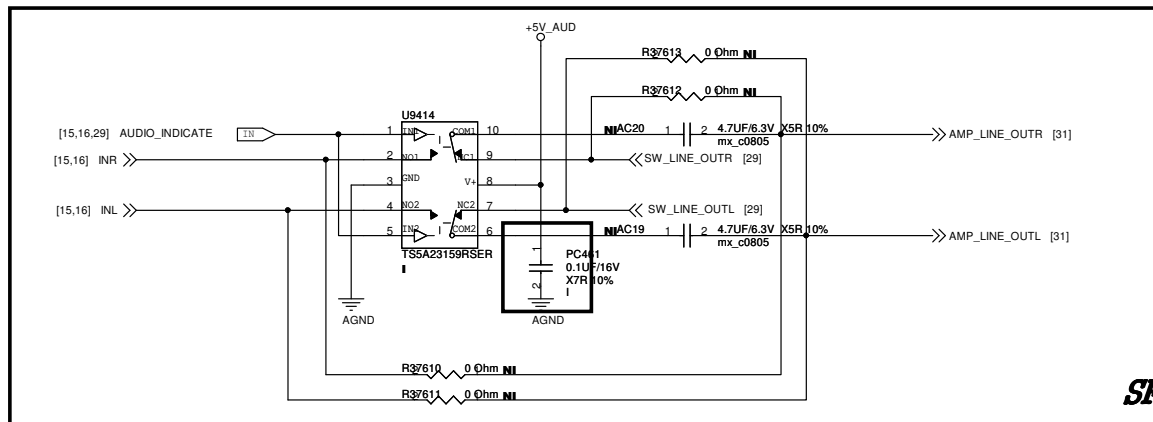


SFA1.02



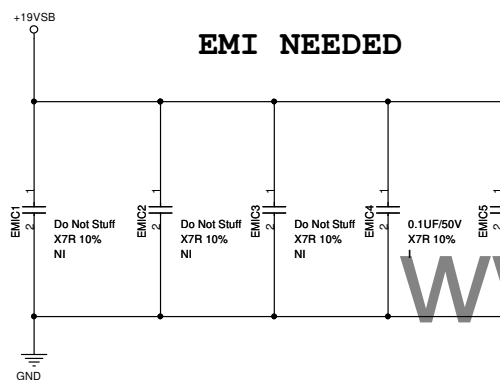
SFA1.02

PEGATRON Title : Amp TPA3100D2			
PEGATRON CORPORATION		Engineer: Jerry, Hsuan	
Size	Project Name		Rev
A3	IPPSB-FA		1.01
Date: Wednesday, April 27, 2011		Sheet	31 of 79

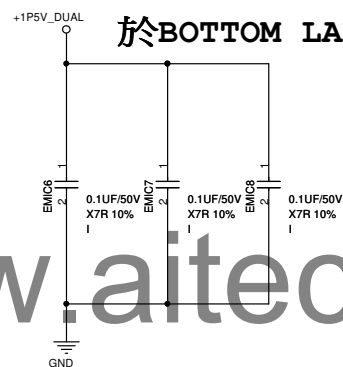


SFA1.04

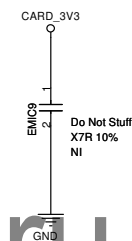
EMI NEEDED



於BOTTOM LAYER 上

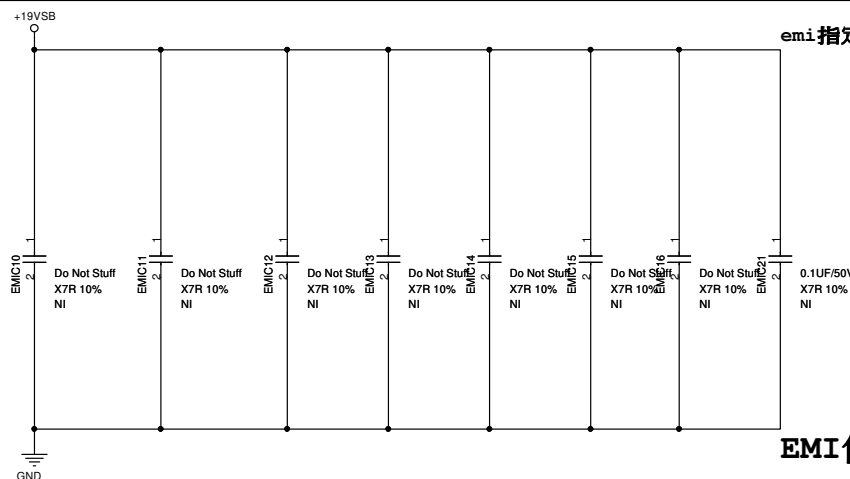


於TOP LAYER 上



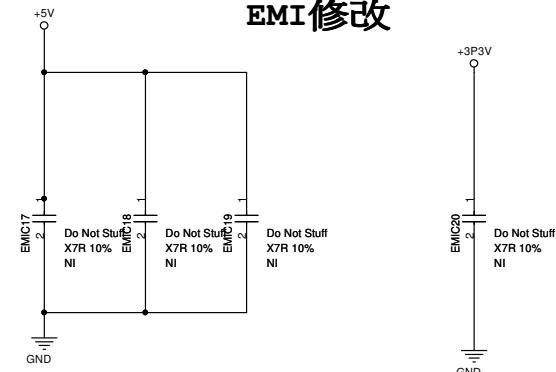
www.aitech1.ru

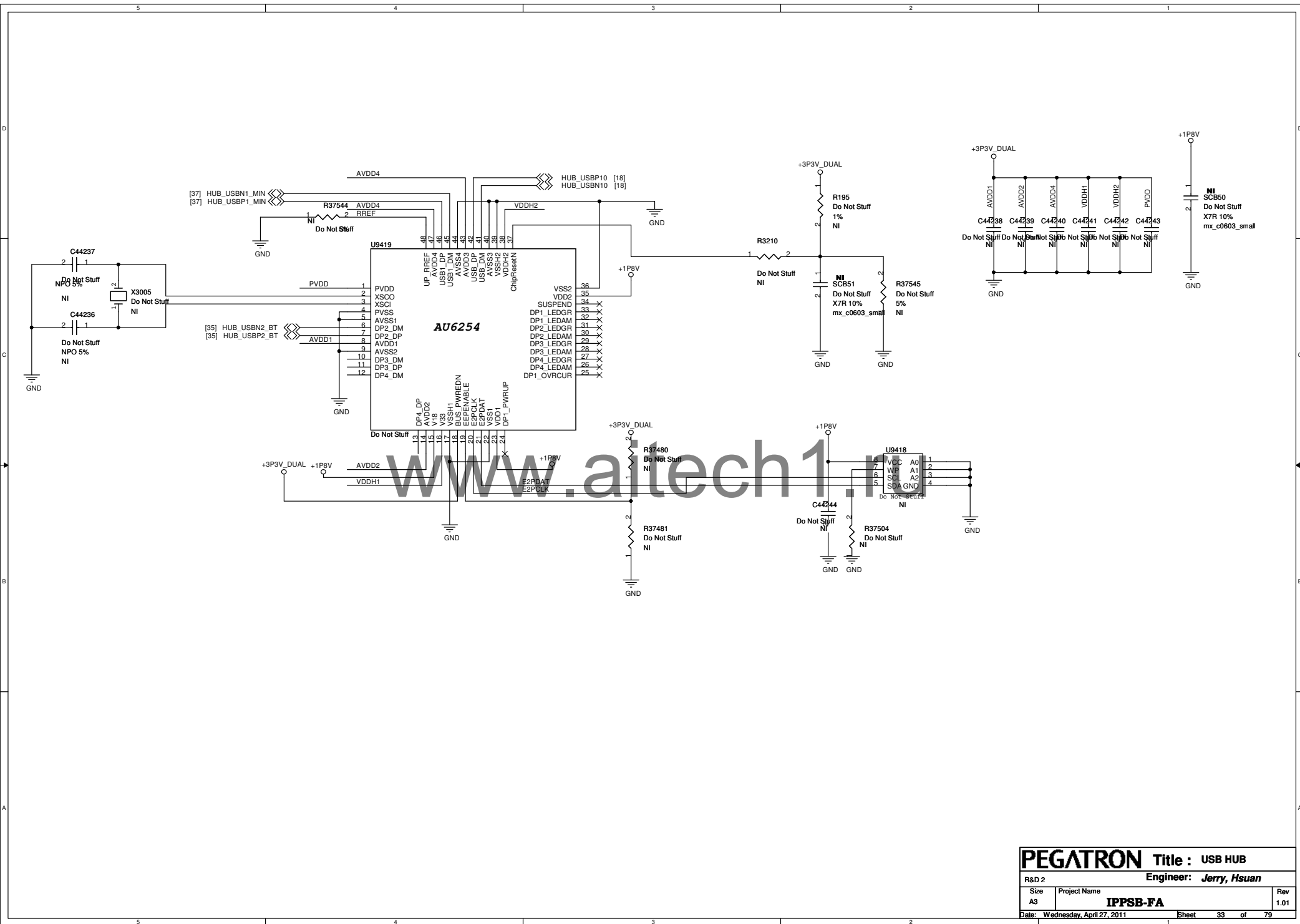
emi指定位置



EMI修改

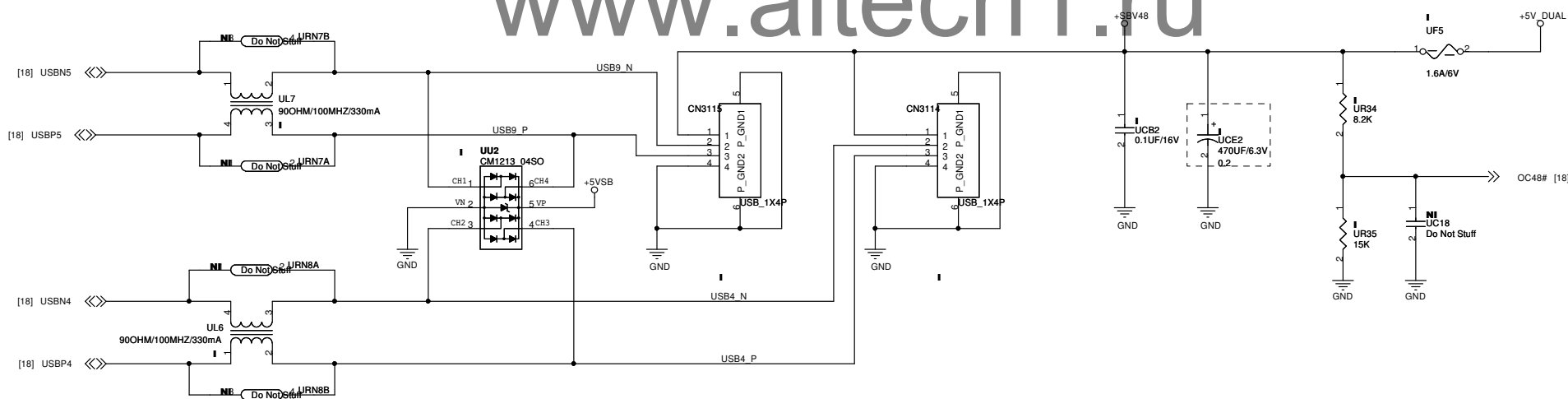
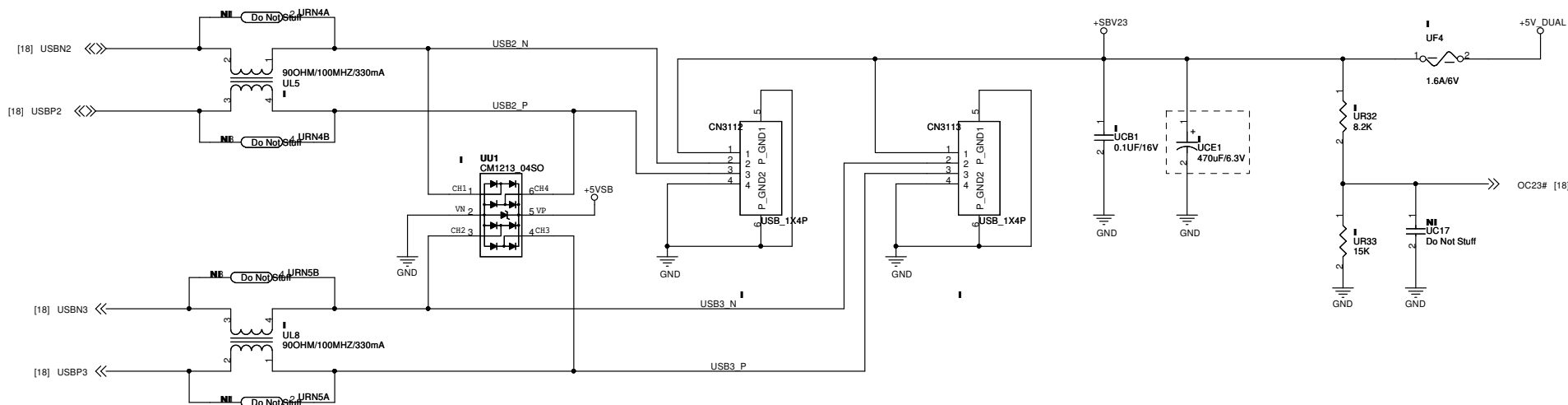
EMI修改





整頁修改過

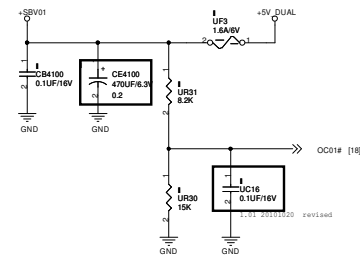
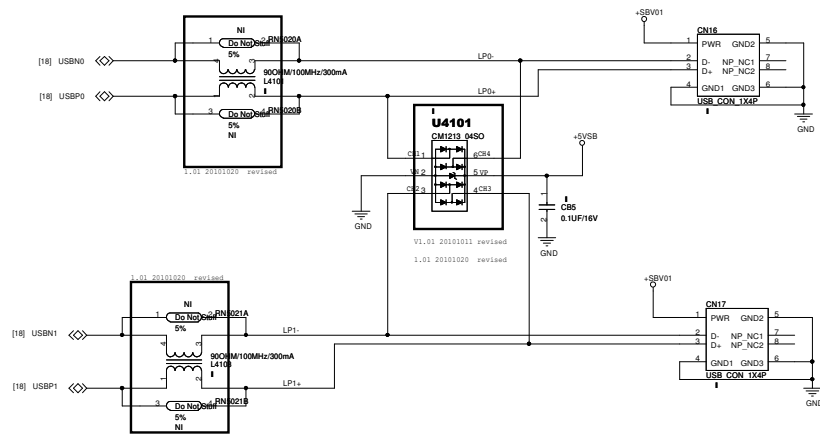
Rear USB2.0 *4



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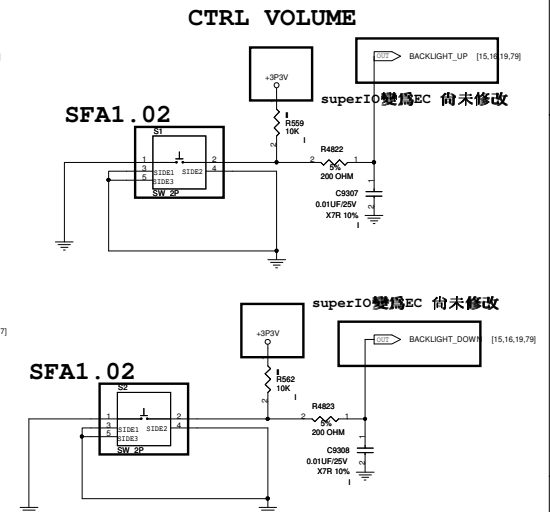
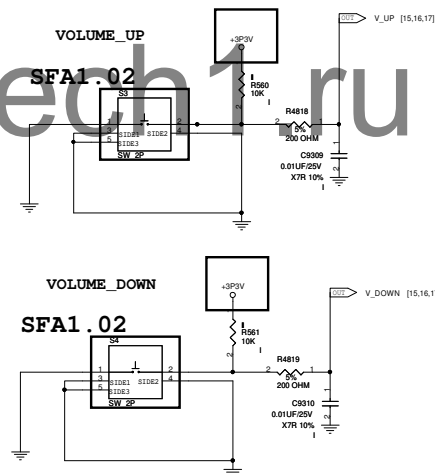
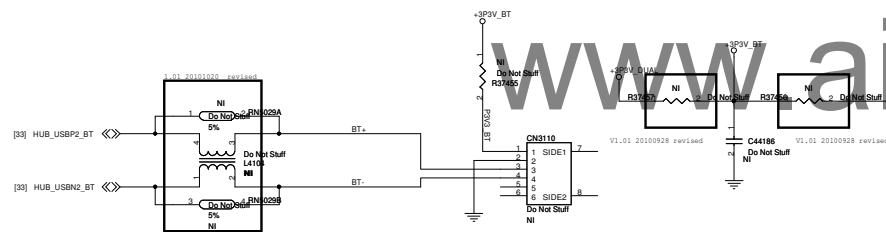
PEGATRON		Title : Rear USB	
PEGATRON CORPORATION		Engineer: Mike Yen	
Size	Project Name	Rev	
A3	IPPSB-FA	1.01	
Date: Wednesday, April 27, 2011		Sheet	34 of 79

已修改過

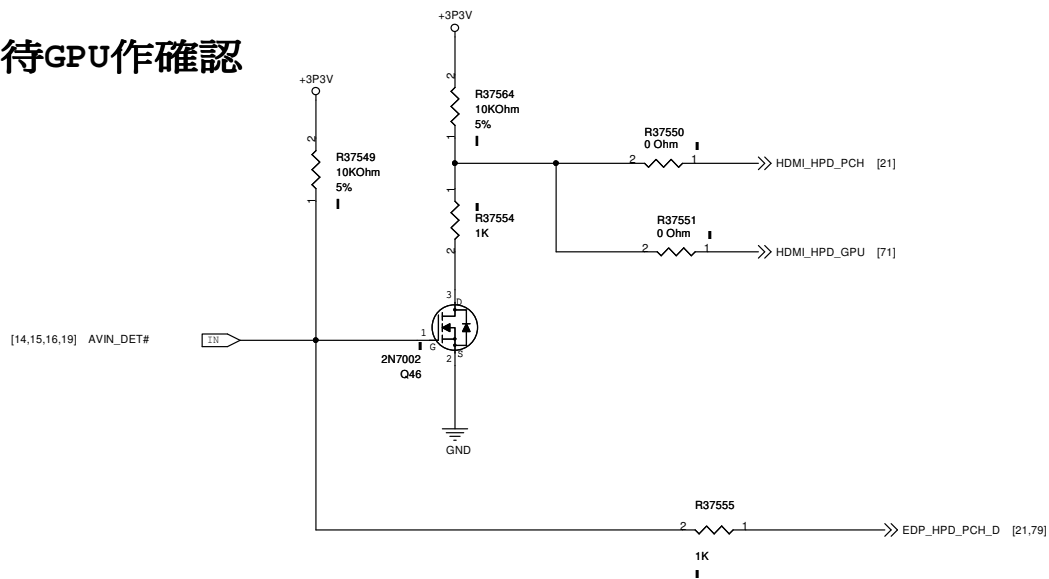


另外增加
Internal I/O
BLUE TOOTH

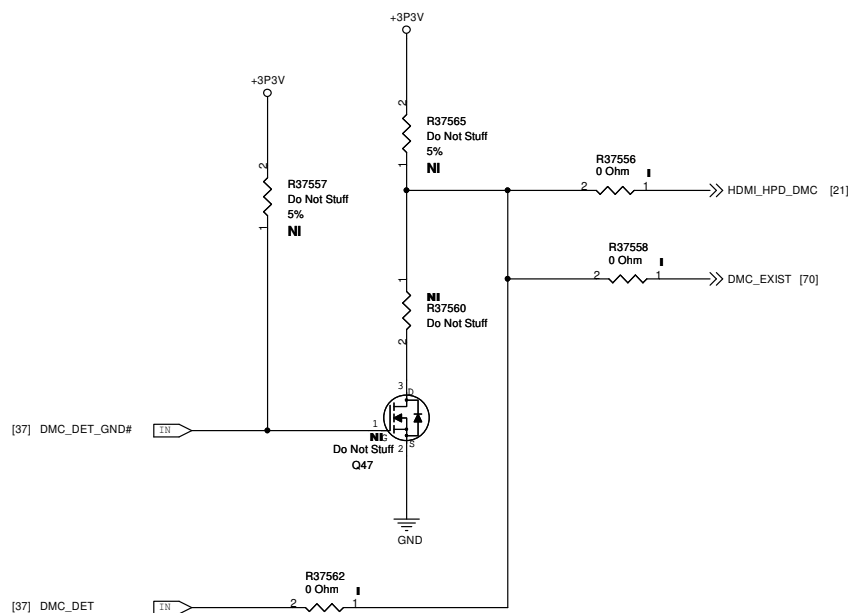
the DMC device connected BT symbols is needed



待GPU作確認



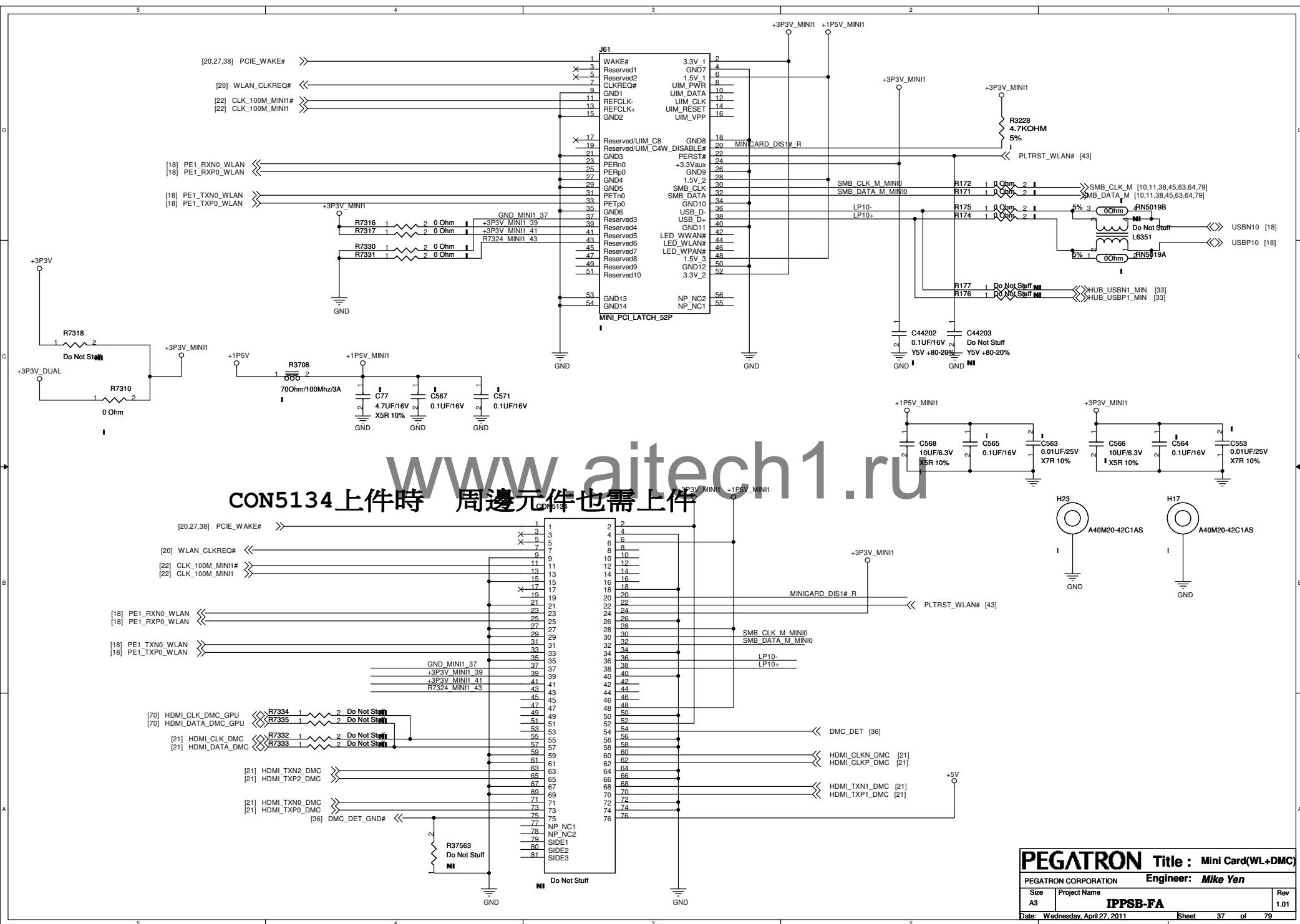
www.aitech1.ru

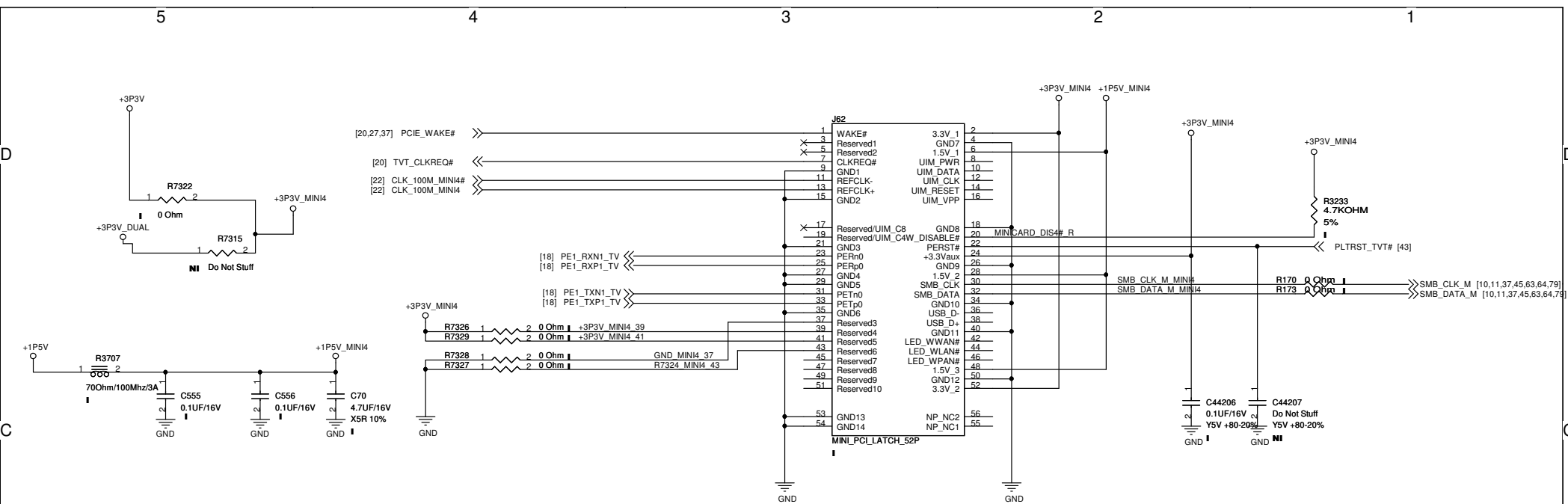


0413

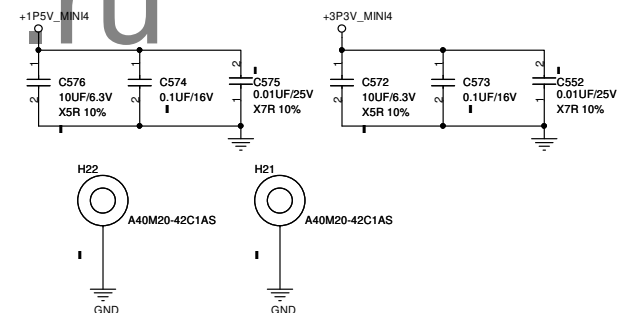
PEGATRON		Title : HPD DET	
R&D 2	Size A3	Project Name IPPSB-FA	Rev 1.01
Date: Wednesday, April 27, 2011		Sheet 36	of 79

Engineer: Jerry, Hsuan





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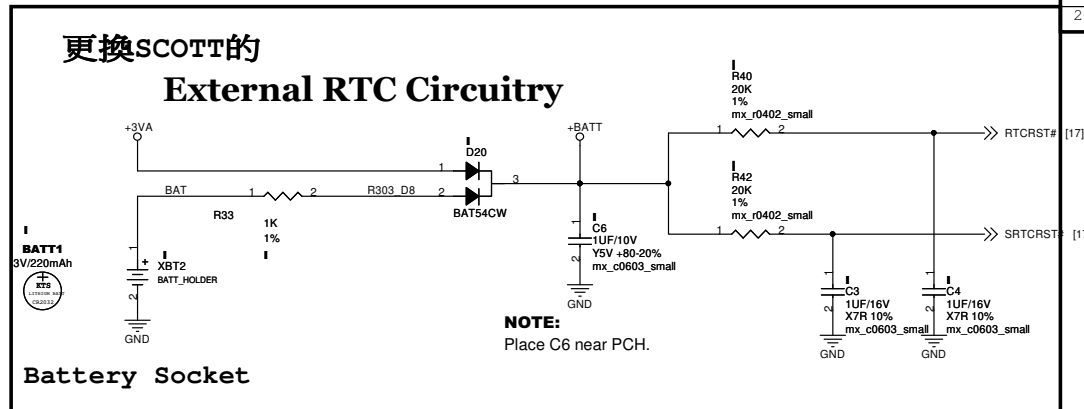


0413

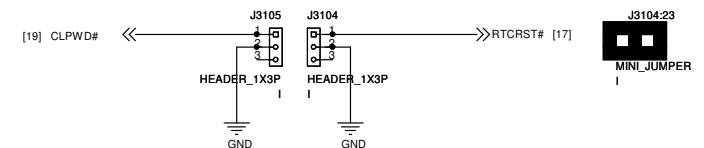
PEGATRON		Title : Mini Card(TVT)	
PEGATRON CORPORATION		Engineer: Mike Yen	
Size	Project Name	Rev	
A3	IPPSB-FA	1.01	
Date: Wednesday, April 27, 2011		Sheet	38 of 79

CLR CMOS CIRCUIT

CLR PASSWORD CIRCUIT

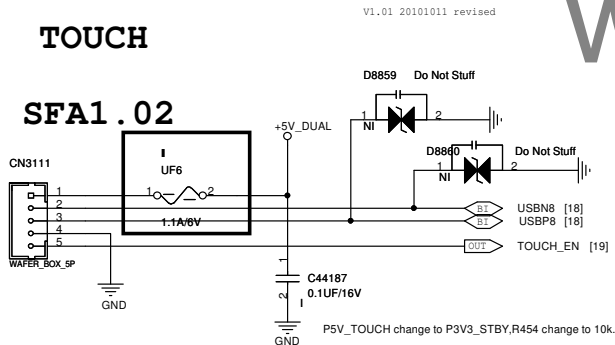


	PASSWORD
1-2	CLEAR
2-3	Default

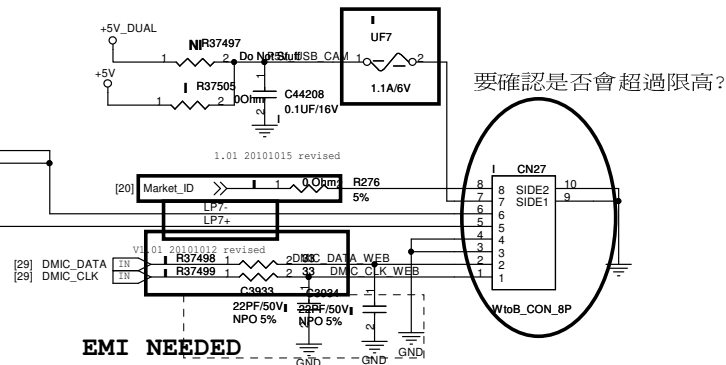


	CMOS RTC
1-2	CLEAR
2-3	Default

TOUCH

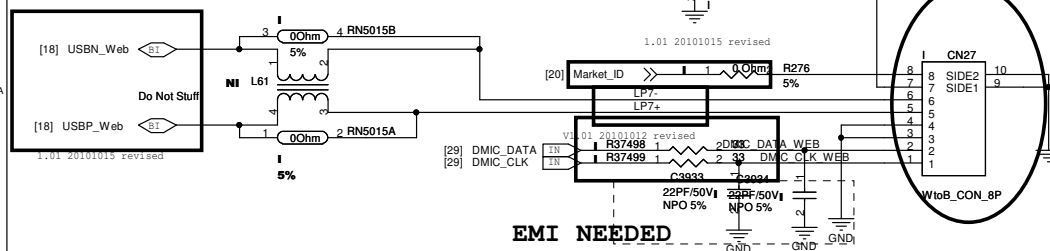


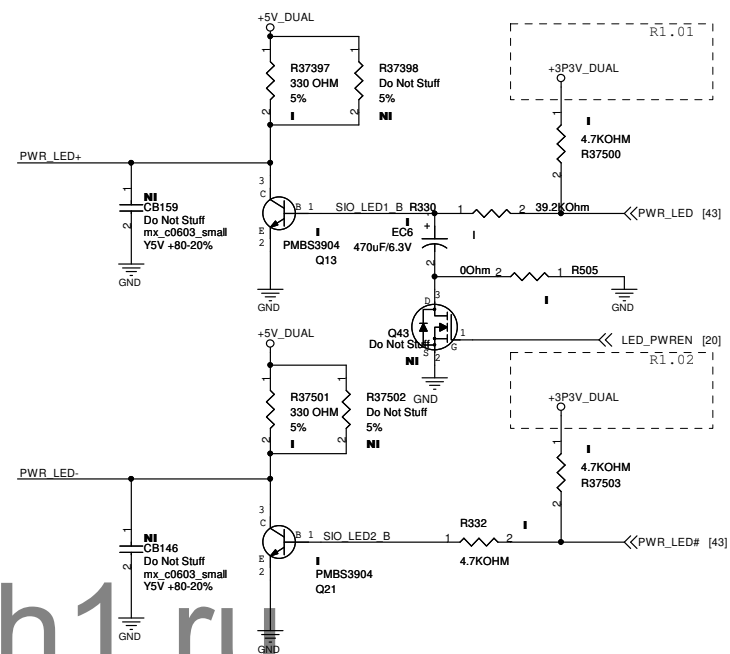
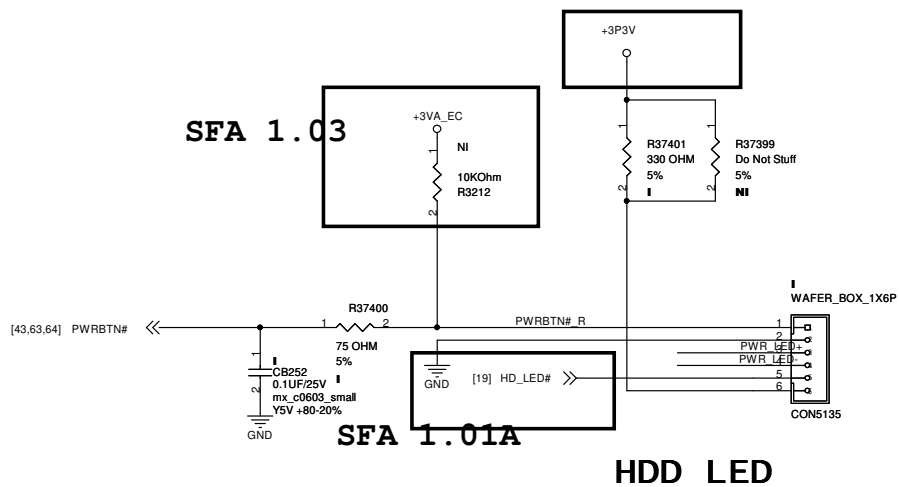
SFA1.03



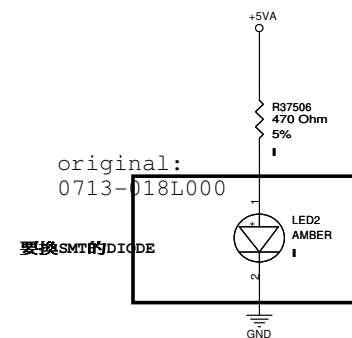
已修改過

AMERA MODULE





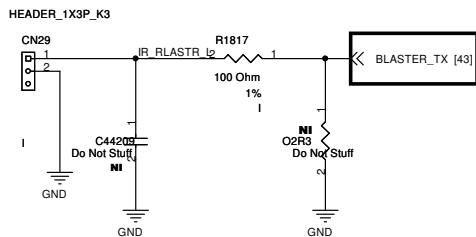
Power supply LED



0413

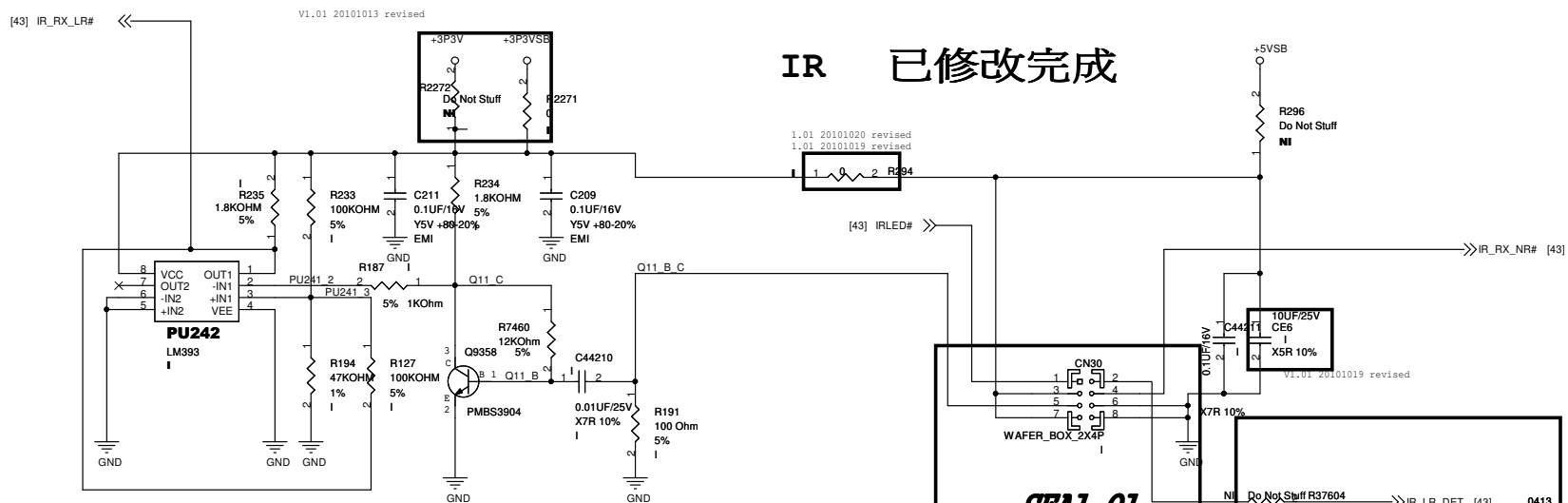
PEGATRON		Title : PWE LED	
PEGATRON CORP.		Engineer: Mike Yen	
Size A3	Project Name IPPSB-FA		Rev 1.01
Date: Wednesday, April 27, 2011		Sheet 41 of 79	

線條未改 IR Blaster



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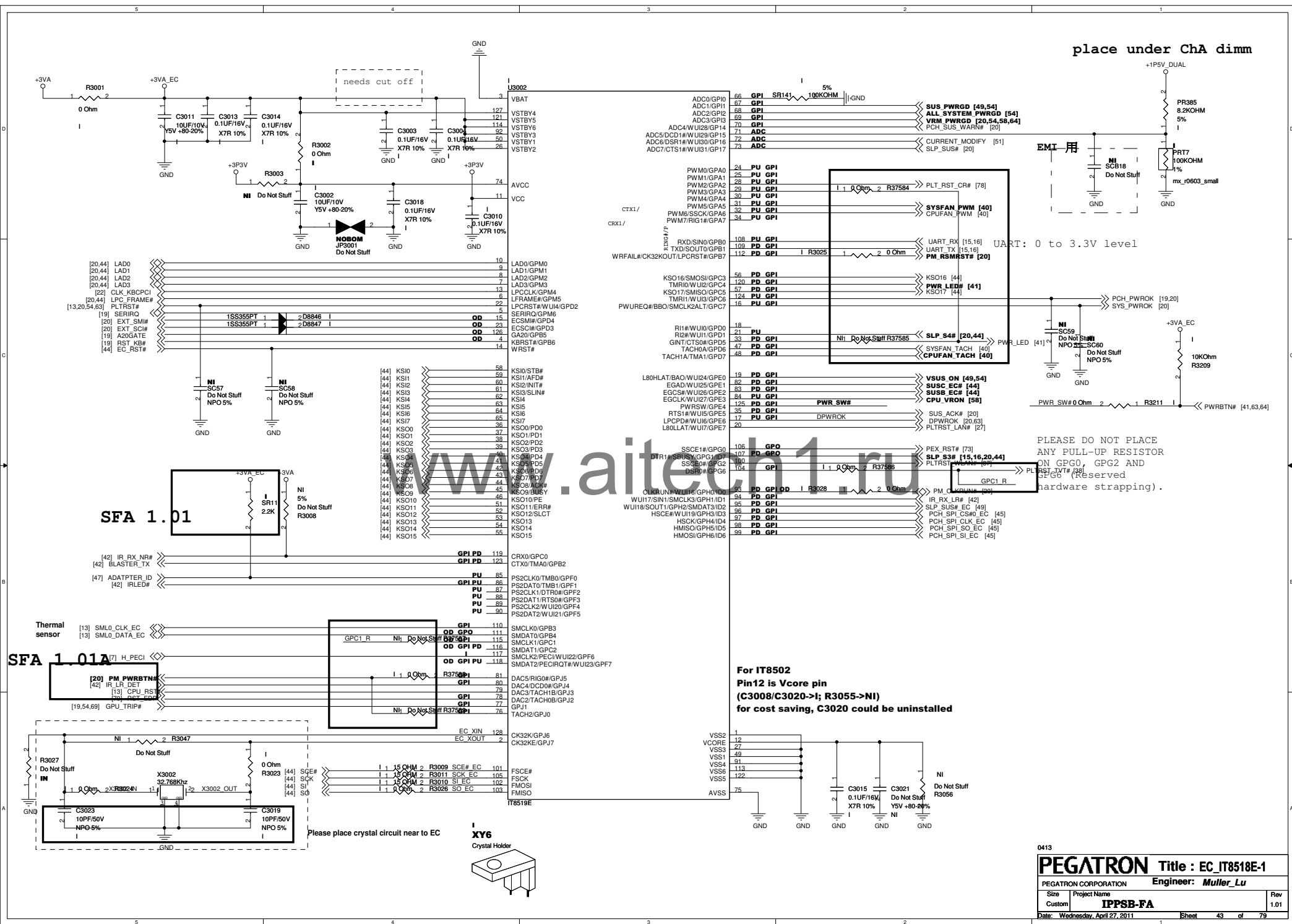
IR 已修改完成



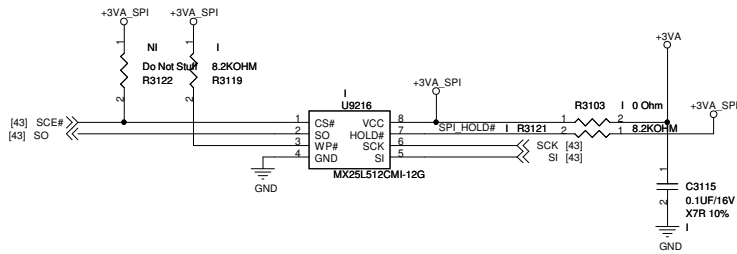
SFA1.01

SFA1.01A

PEGATRON		Title : IR LEDs	
PEGATRON CORPORATION		Engineer: Mike Yen	
Size A3	Project Name IPPSB-FA	Rev 1.01	
Date: Wednesday, April 27, 2011		Sheet 42 of 79	



SPI ROM+ External programming conn.

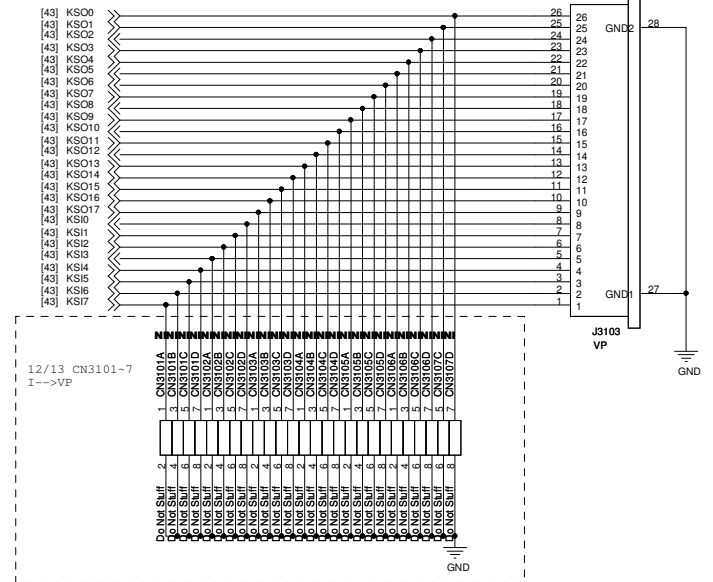


Touch PAD(deleted)

For Instant Key & Switch

Note: Close to EC

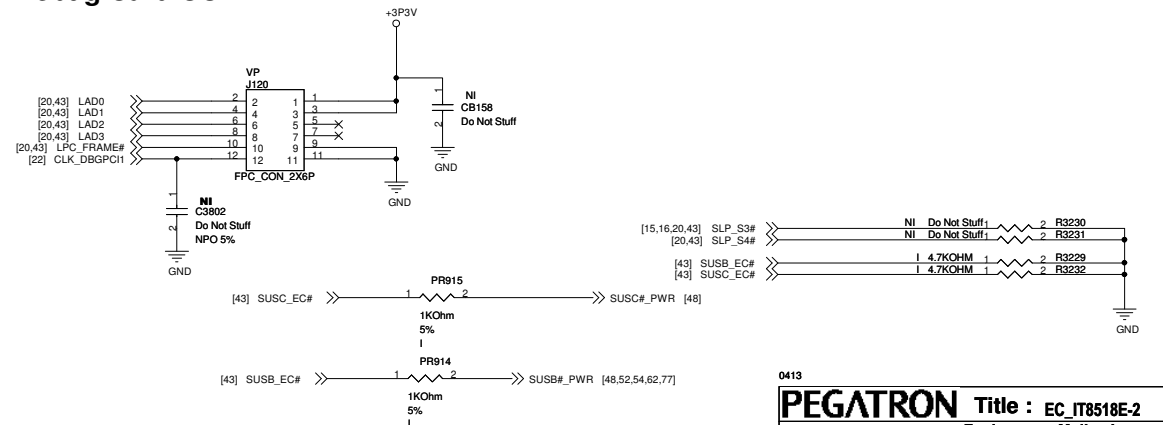
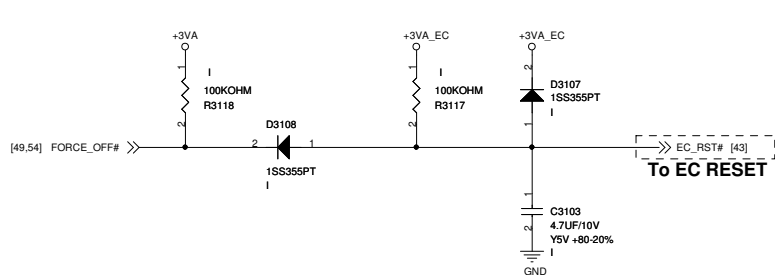
Keyboard Connector(debug)



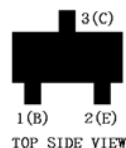
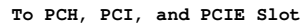
www.aitech1.ru

For EC PU/PD

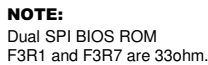
Debug Card CON



SM BUS Control



SPI BIOS ROM - 64 Mb or 32Mb



64Mb: 05X00Z2GE330

NOTE:
Dual SPI BIOS ROM
F3R5 and F3R6, F3R8 and F3R9 are 33ohm

PEGATRON DT-MB RESTRICTED SECRET

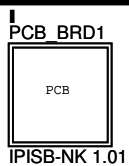
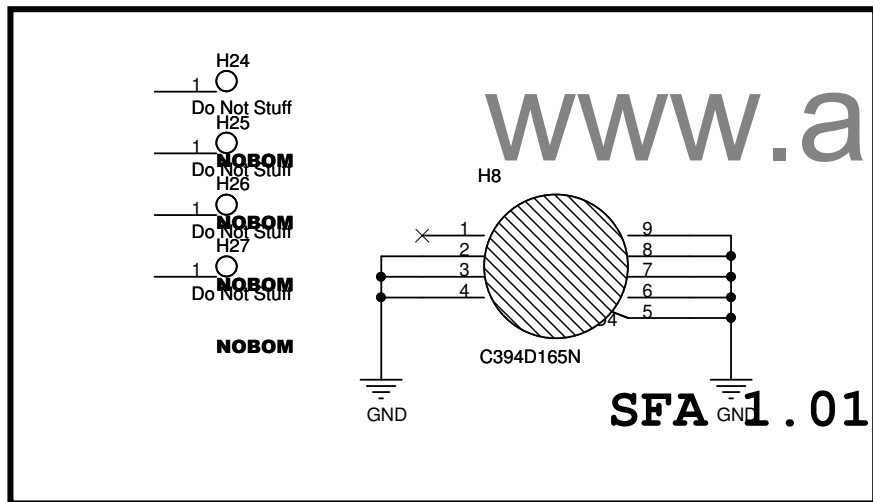
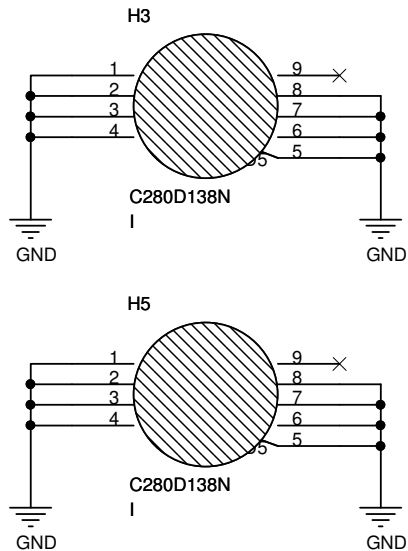
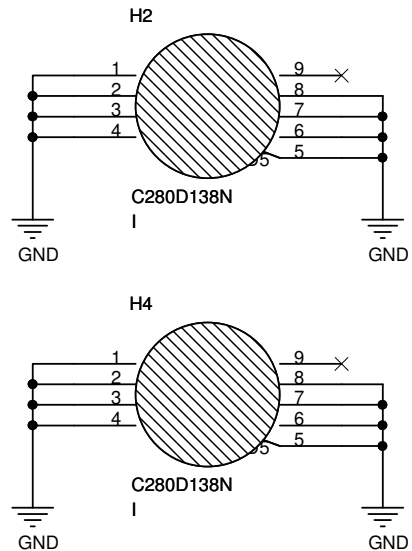
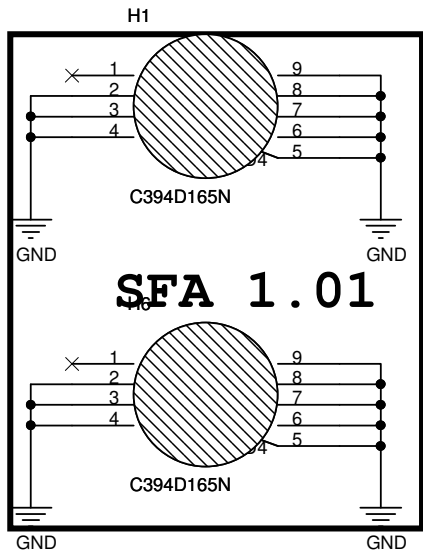
PEGATRON Title : SM BUS & SPI RO

PEGATRON CORPORATION **Engineer:** **XXXX-XX**

Size	Project Name	Re
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A3	IPFSB-FA	1.0
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VESA mount hole

0413

PEGATRON		Title : SCREW HOLE	
PEGATRON CORPORATION		Engineer: Mike Yen	
Size A	Project Name IPPSB-FA		Rev 1.01
Date: Wednesday, April 27, 2011		Sheet	46 of 79

change to SIMULA /AJ261B-Y090-42F, p/n applying....

H/L

J121

S1 P_GND

S2 P_GND

S3 P_GND

1 (+) SPRING

2 (-) SPRING

P1 NP_NC1

P2 NP_NC2

P3 NP_NC3

S4 SIGNAL

ADAPTER_ID [43]

DC_POWER_JACK_3P

C9365

Do Not Stuff

X7R 10%

NI

GND

+19VA_VIN

L6322 1

2 70Ohm/100Mhz/3A

L6323 1

2 70Ohm/100Mhz/3A

L6324 1

2 70Ohm/100Mhz/3A

PC233

0.1UF/50V

GND

+19VA

PC232

1UF/50V

GND

+19VA_SN_A

PR181

Do Not Stuff

5%

NI

PR190

Do Not Stuff

5%

NI

PR191

Do Not Stuff

5%

NI

PR192

100 Ohm

5%

NI

+19VA_SN

PR9209

200K

1%

PC1003

1UF/16V

mx_c0603_small

X7R 10%

+19VSB_HB C

Q9350

TPC8107

1

2

3

4

5

6

7

8

+19VSB_R

D8814

SS14

GND

+19VA

PR9210

100KOHM

1%

Q115

2N7002

1

2

3

GND

+19VA

PR112

100K

1%

PR186

49.9K

1%

PC206

1000PF/50V

X7R 10%

GND

H/L

OVP#

Q117

2N7002

1

2

3

GND

+19V_OV_A

UVP#

Q116

2N7002

1

2

3

GND

+19V_UV_A

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OVP

~24V

PR9211

40.2KOHM

1%

PD110

BAT54AW

1

2

3

PR9212

4.7KOHM

1%

GND

PR9211

BAT54AW

1

2

3

PC200

1000PF/50V

X7R 10%

PC201

10UF/6.3V

X7R 10%

GND

GND

PU110

LM393

1

2

3

4

5

6

7

8

OUT1

-IN1

VCC

OUT2

-IN2

VEE

+IN1

+IN2

GND

+19VA_SN_A

UVP#

PR101

243KOHM

1%

UVP REF

UVP1_REF

PR97

1K

1%

PR99

100KOHM

1%

PR96

100K

1%

PR9213

18.2KOHM

1%

PC236

1000PF/50V

X7R 10%

PR9214

49.9K

1%

GND

GND

GND

+19VA

PR287

10K

1%

PR435

Do Not Stuff

1%

NI

Q259

H431BN

1

2

3

GND

+2PSVREF

PC203

10UF/6.3V

XSR 10%

GND

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : UVP, OVP & +19VSB

PEGATRON CORPORATION Engineer: Mike Yen

Size Project Name

A3 IPPSB-FA

Date: Wednesday, April 27, 2011 Sheet 47 of 79 Rev 1.01

change to SIMULA /AJ261B-Y090-42F, p/n applying....

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PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : UVP, OVP & +19VSB

PEGATRON CORPORATION Engineer: Mike Yen

Size	Project Name	Rev
A3	IPPSB-FA	1.01

Date: Wednesday, April 27, 2011 Sheet 47 of 79

change to SIMULA /AJ261B-Y090-42F, p/n applying....

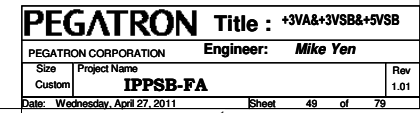
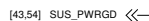
www.aitech1.ru

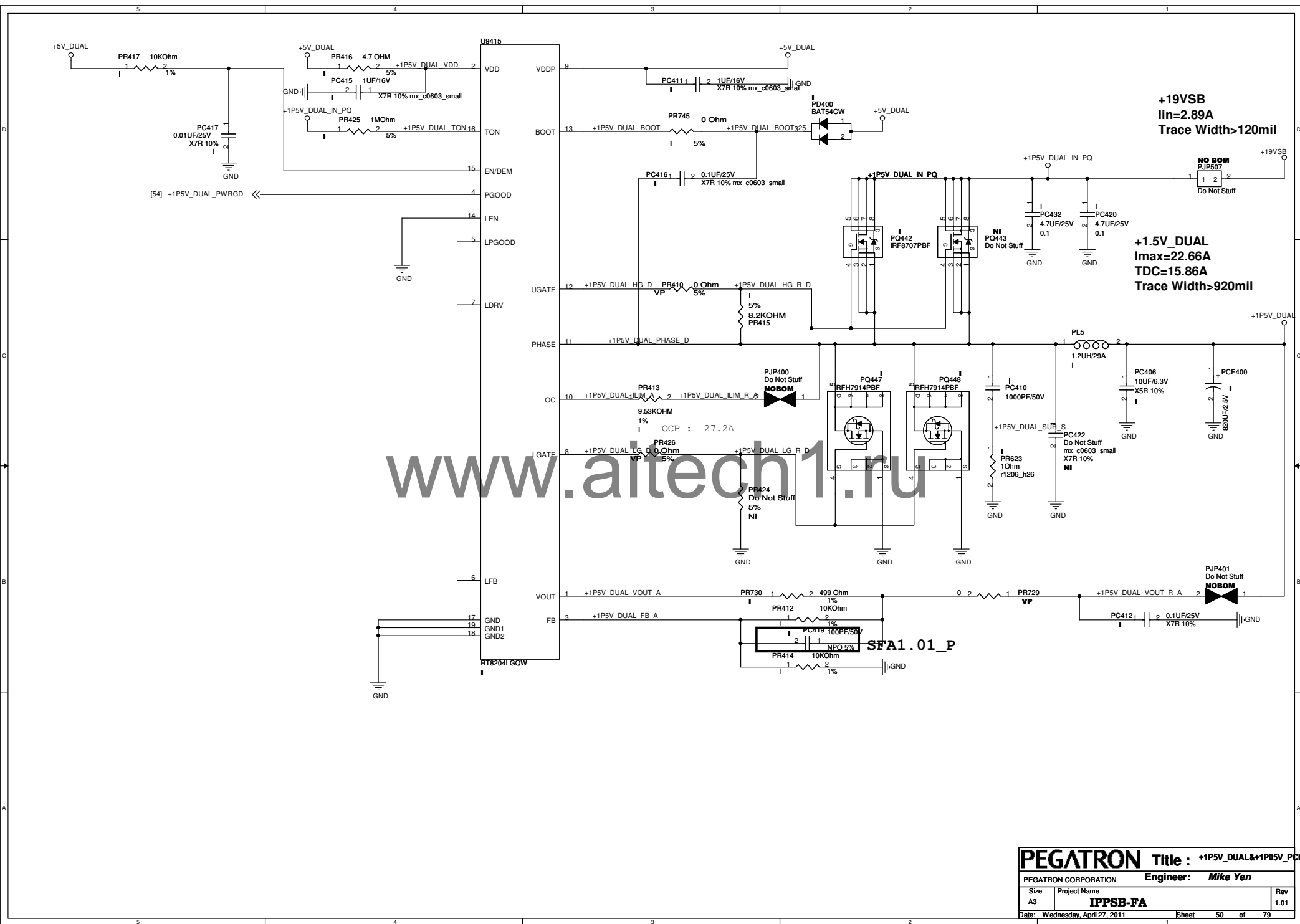
PEGATRON DT-MB RESTRICTED SECRET

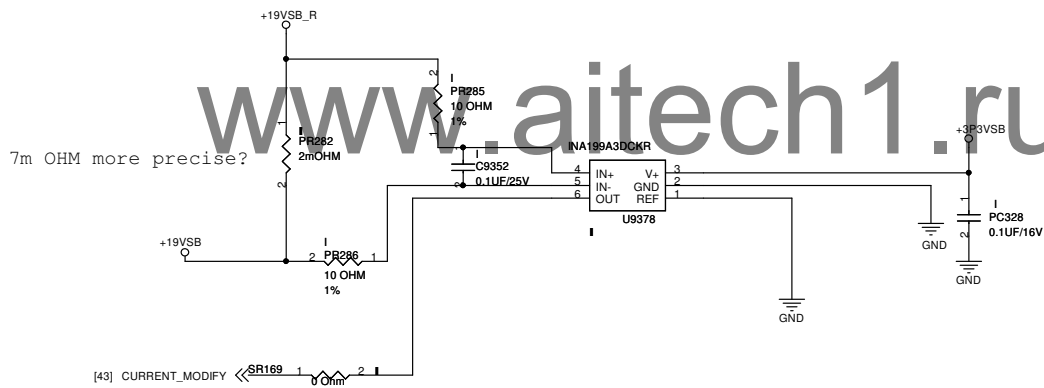
PEGATRON Title : UVP, OVP & +19VSB

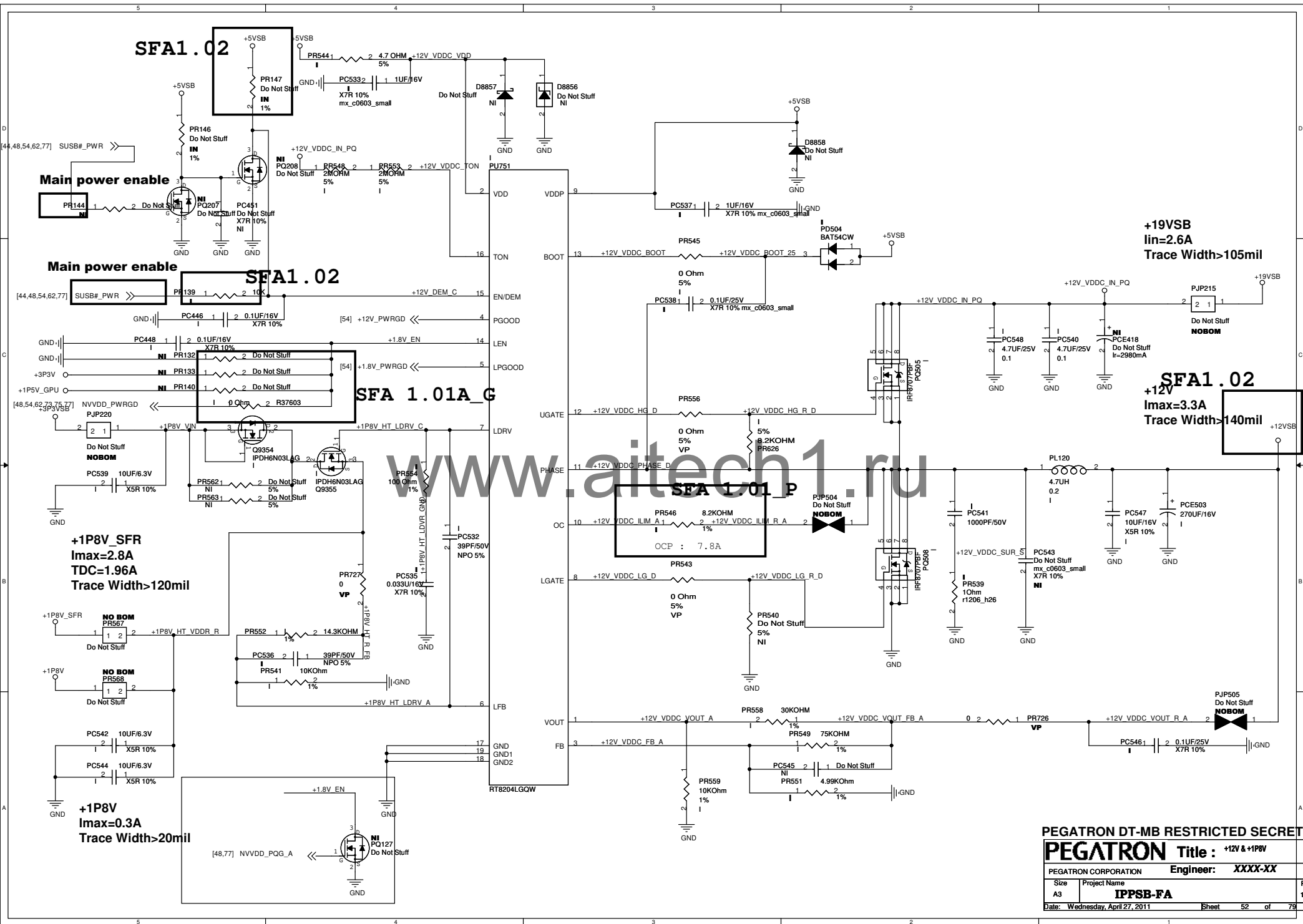
PEGATRON CORPORATION		Engineer: Mike Yen	
Size A3	Project Name IPPSB-FA	Rev 1.01	
Date: Wednesday, April 27, 2011		Sheet 47	of 79

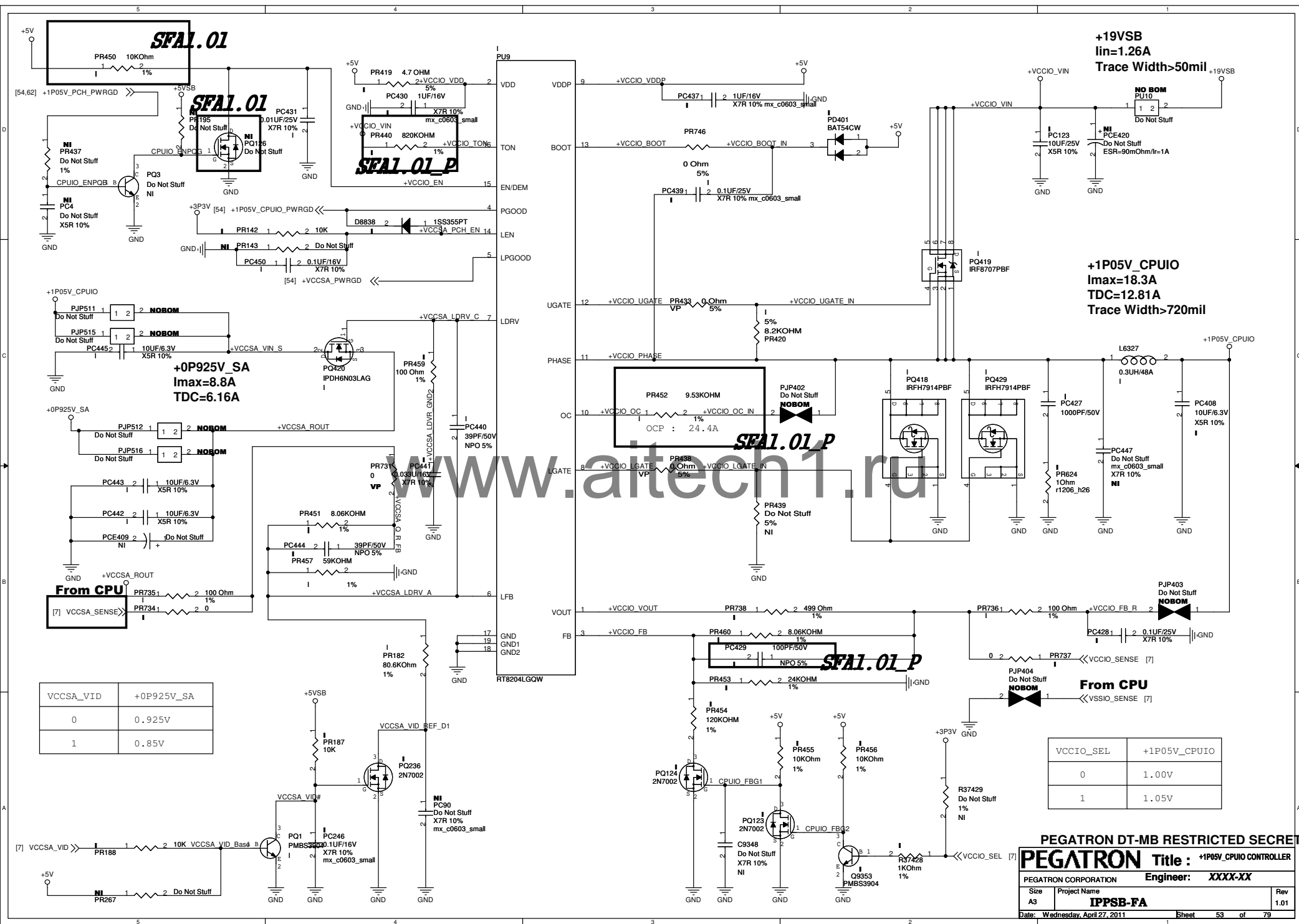
+5VSB
Imax=18.07A
TDC=12.65A
Trace Width>730mil

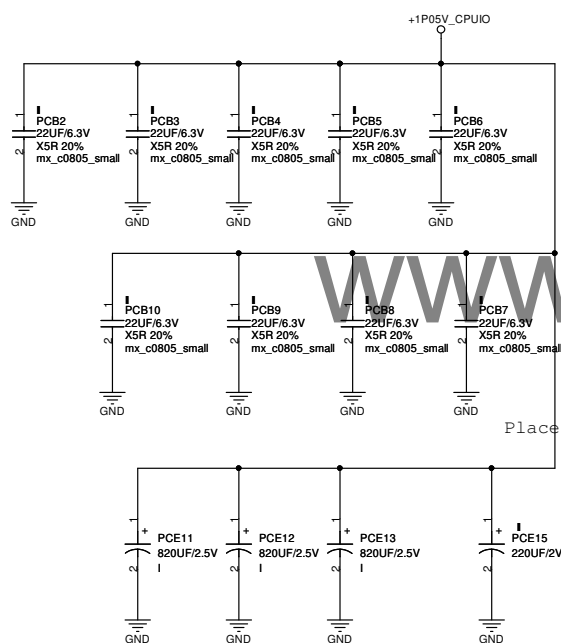
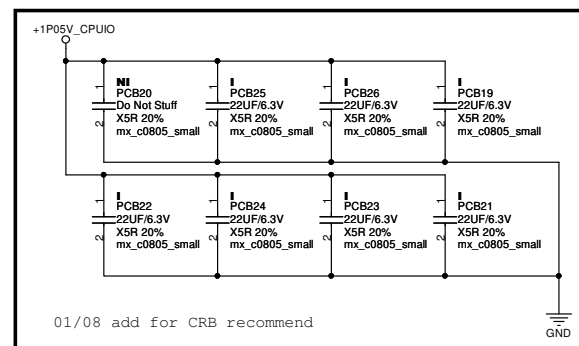
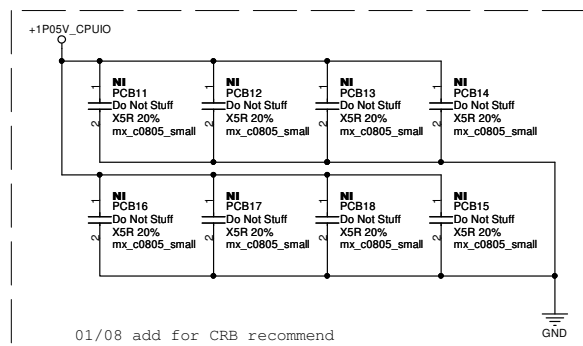












VCCIO Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	3	7mΩ	1.4nH	Output	Various. See layout figures	1
22µF 0805 X5R	9	5mΩ	0.55nH	Output	Inside processor socket cavity	1, 2, 3
0805 placeholders	16				Backside	

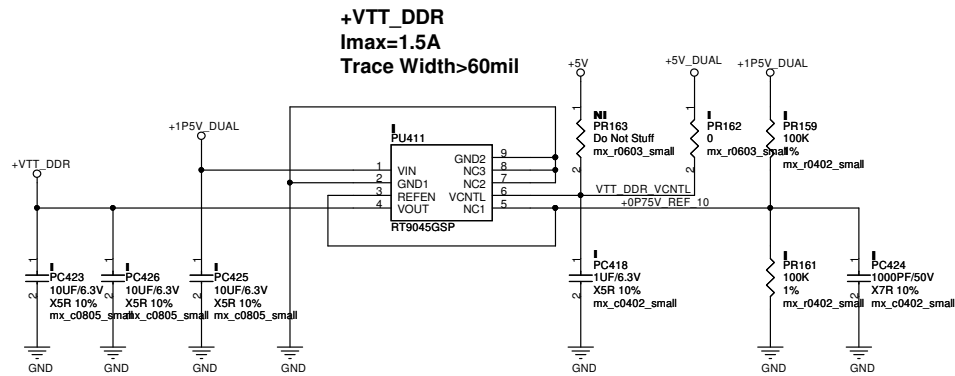
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : 1P05V_CPUIO CAP

PEGATRON CORPORATION Engineer: XXXX-XX

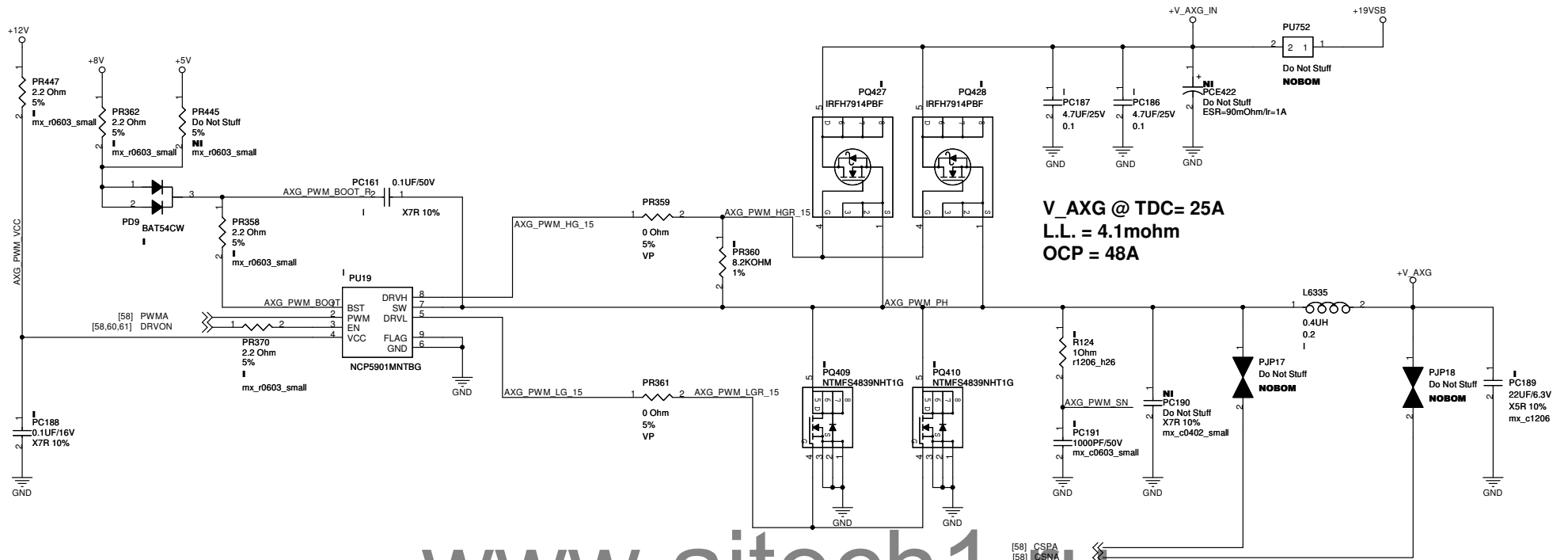
Size A3 Project Name IPSPB-FA Rev 1.01

Date: Tuesday, April 26, 2011 Sheet 55 of 79



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PEGATRON			Title :	+VTT_DDR
PEGATRON CORPORATION			Engineer:	Mike Yen
Size	Project Name			Rev
A3	IPPSB-FA			1.01
Date: Tuesday, April 26, 2011		Sheet	56	of 79

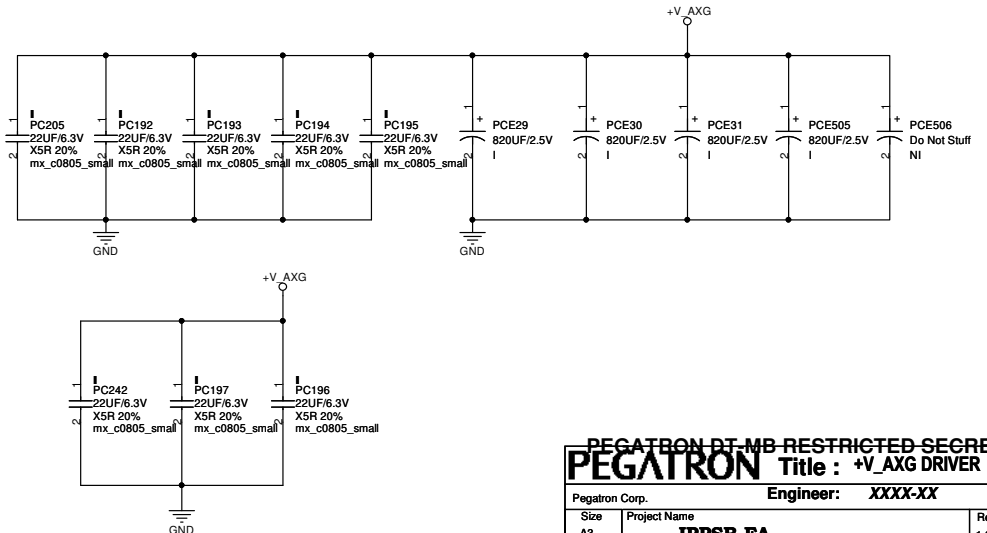


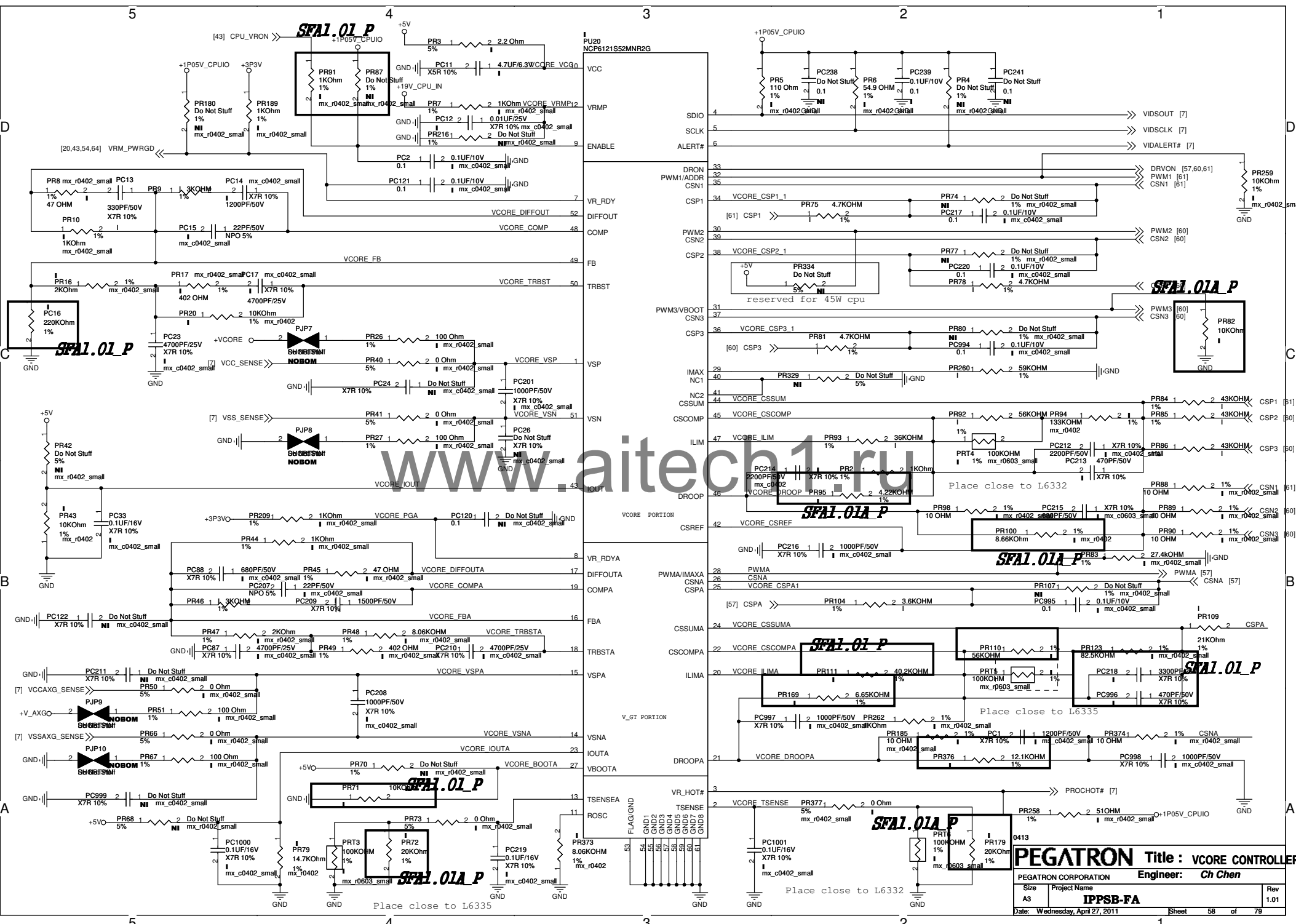
Output CAP

Table 30-4. VCCAXG Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	East of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	6	5mΩ	0.55nH	Output	4 - inside processor socket cavity 2(empty) - Bottom of board, near socket	1, 2, 3
4.7µF X5R	3	7mΩ	0.6nH	Input		1

PL-CAP *4
MLCC *6



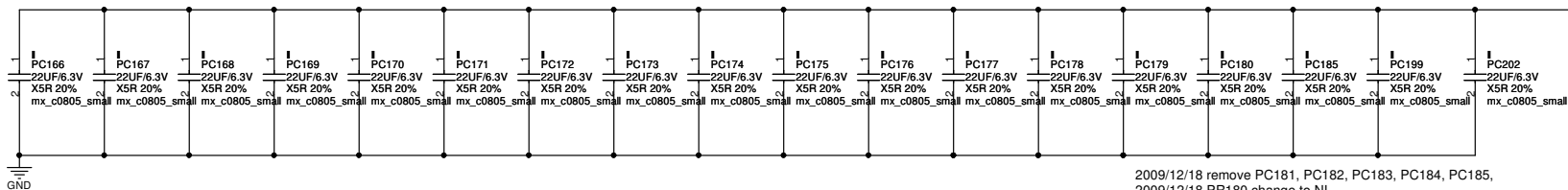
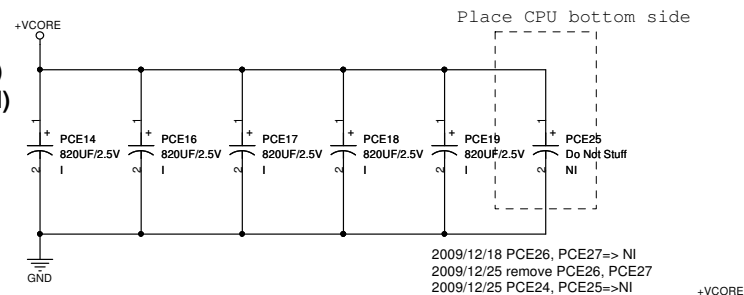


Output CAP

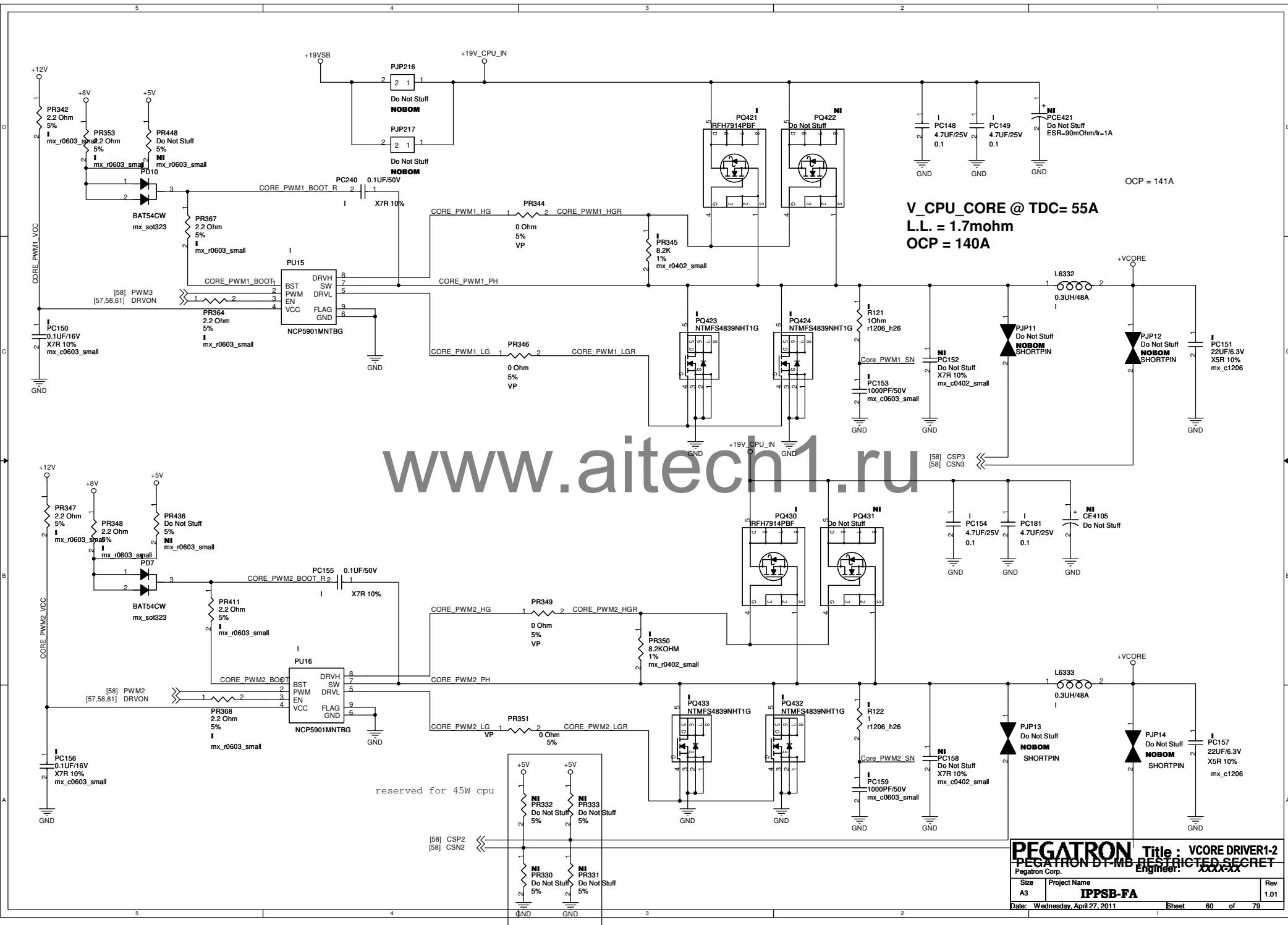
Table 30-2. Decoupling Requirements

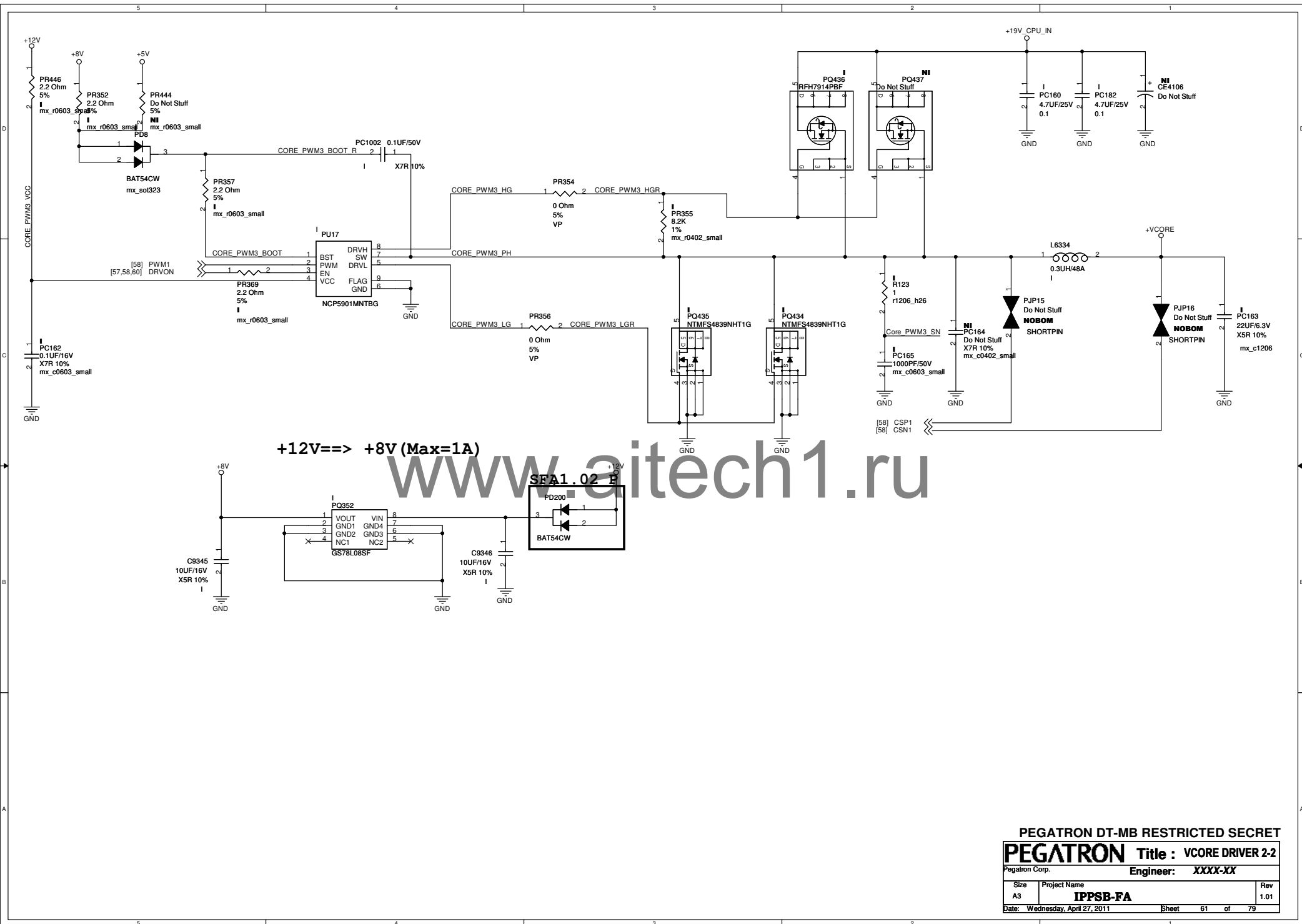
Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	North of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	18	5mΩ	0.55nH	Output	14 - Inside processor socket cavity 4 - North of processor - as close to RM keep-out as possible	1, 2, 3
Aluminum Electrolytic 390µF	4	51mΩ	6.1nH	Input		1
4.7µF X5R	9	7mΩ	0.6nH	Input		1

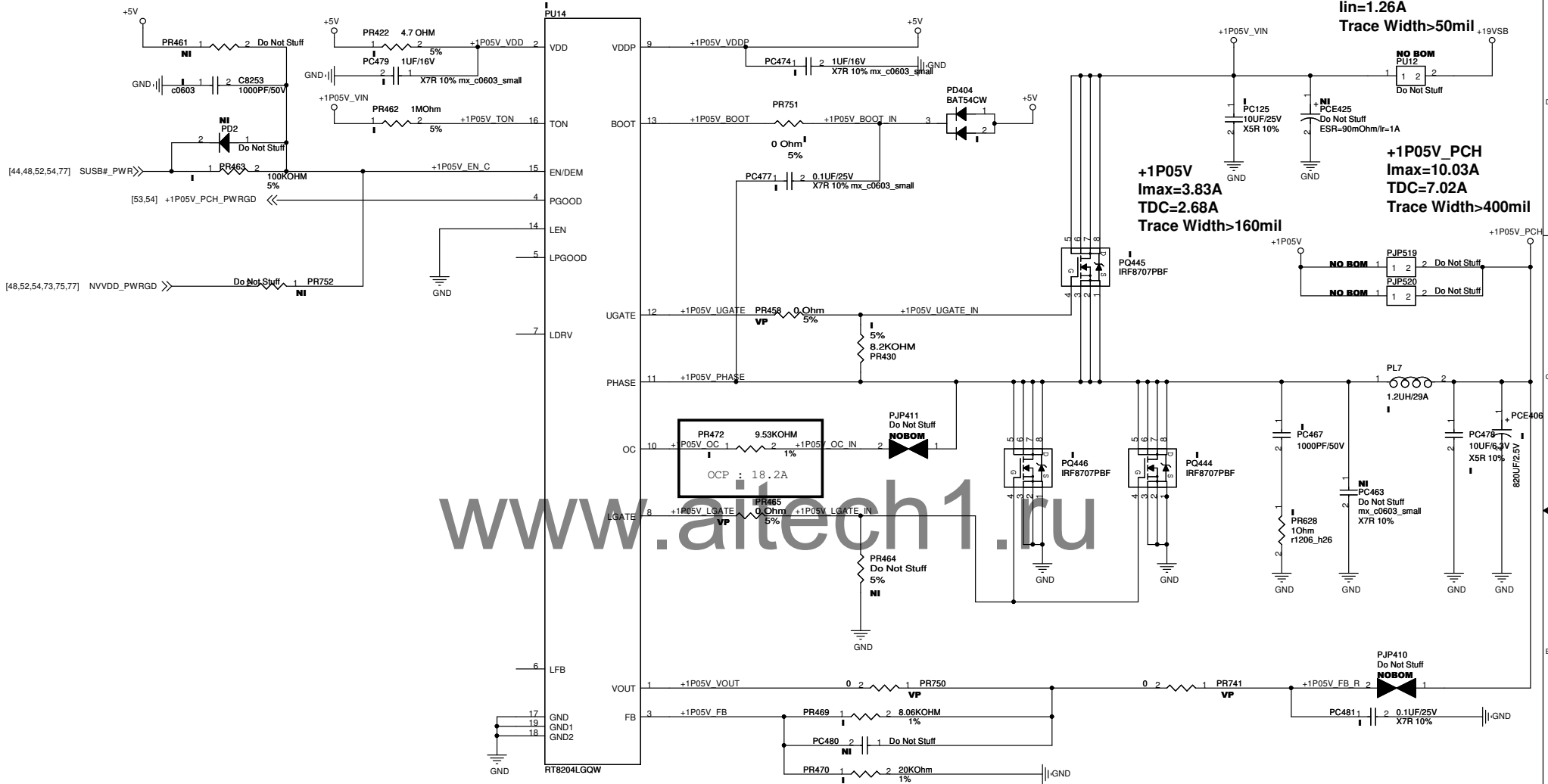
PL-CAP *4 +2(NI)
MLCC *18 +3(NI)



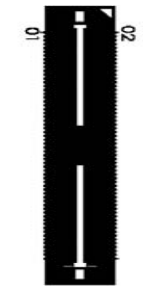
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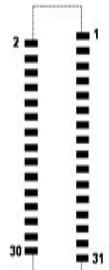




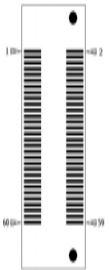
INTEL PCH XDP DEBUG PORT



TOP SIDE VIEW

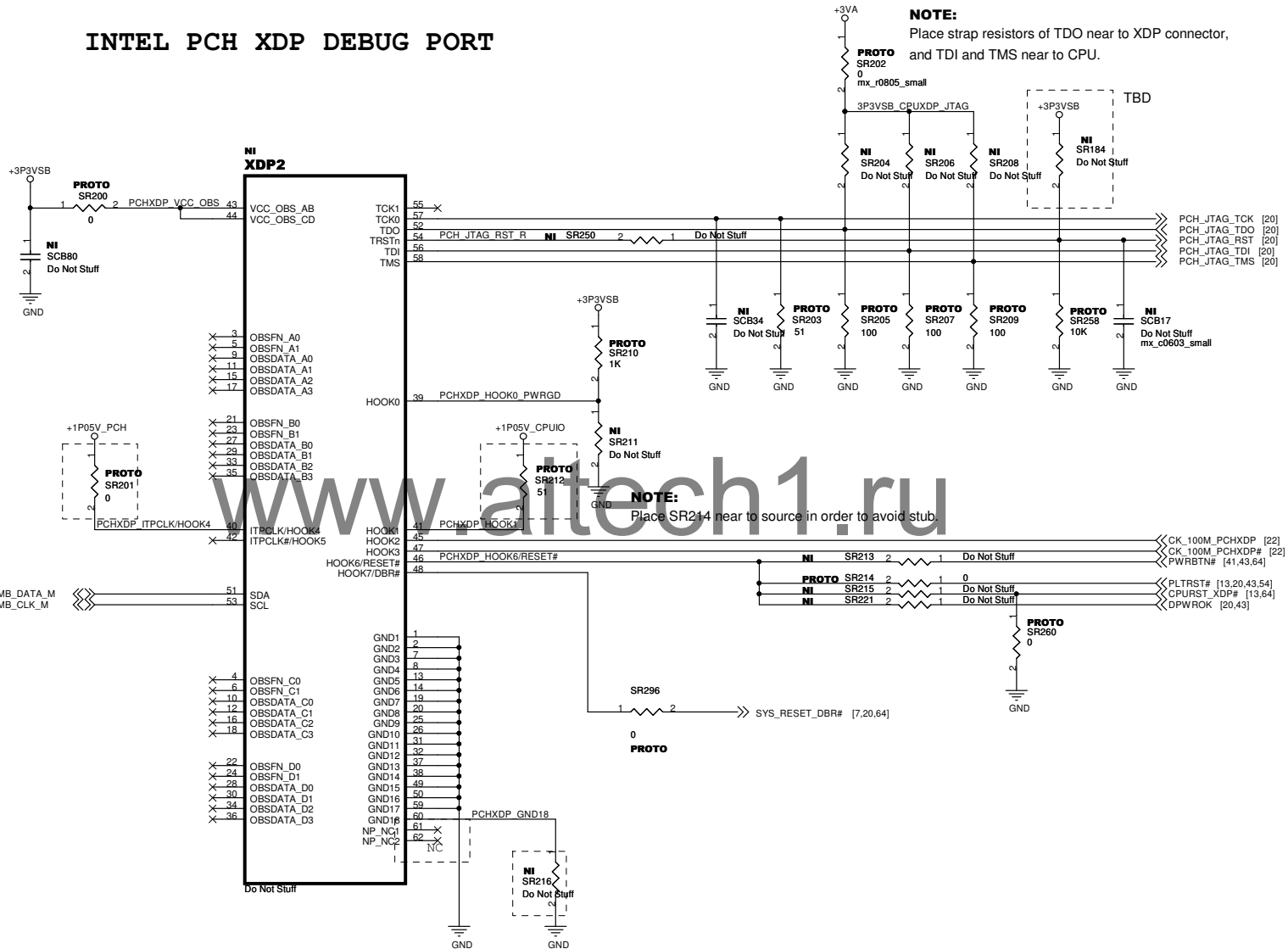


HR8/DF9C-31S-1V(22)
PCB FOOTPRINT



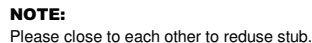
BOTTOM SIDE VIEW

[10,11,37,38,45,64,79] SMB_DATA_M
[10,11,37,38,45,64,79] SMB_CLK_M





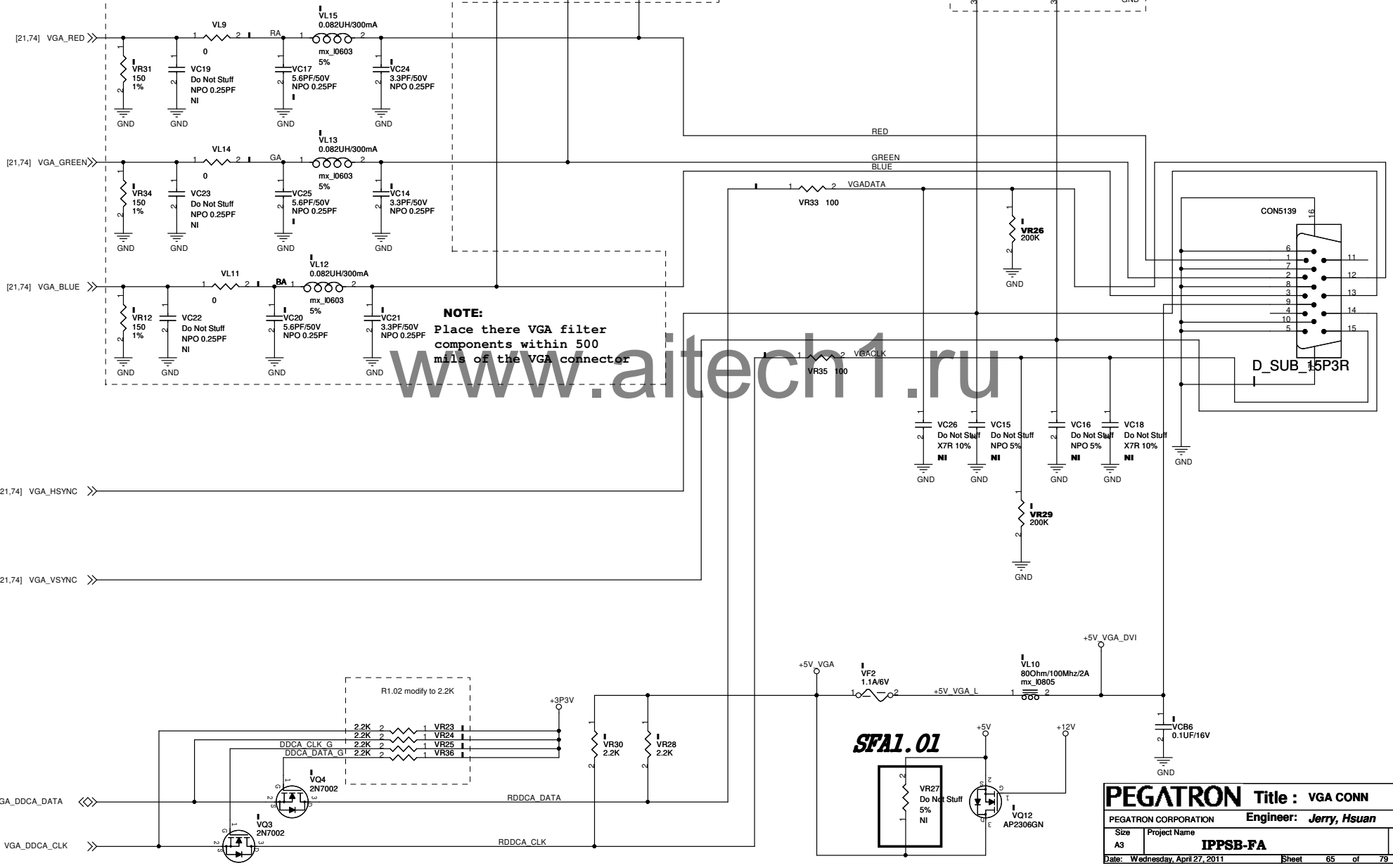
INTEL CPU XDP DEBUG PORT

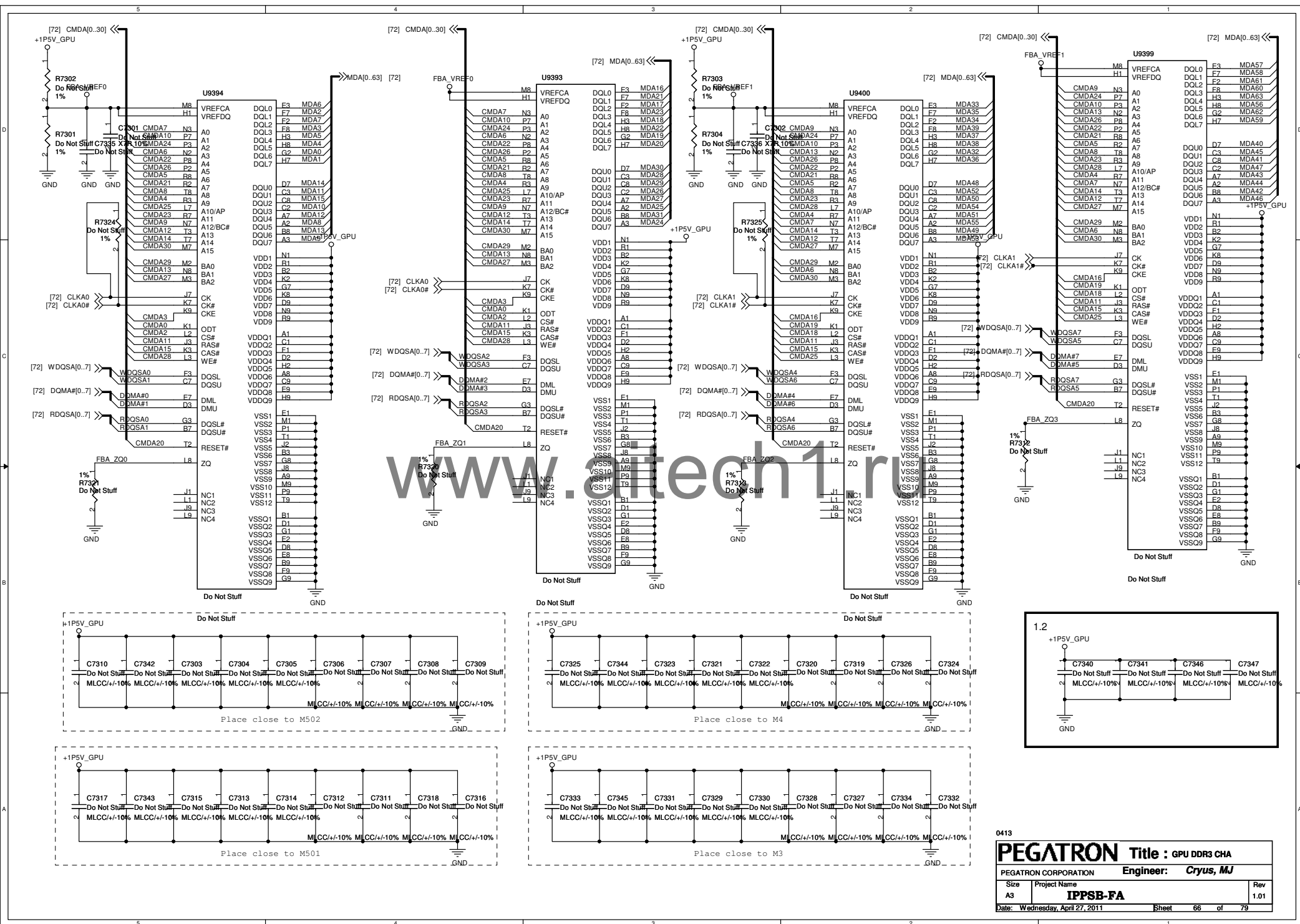


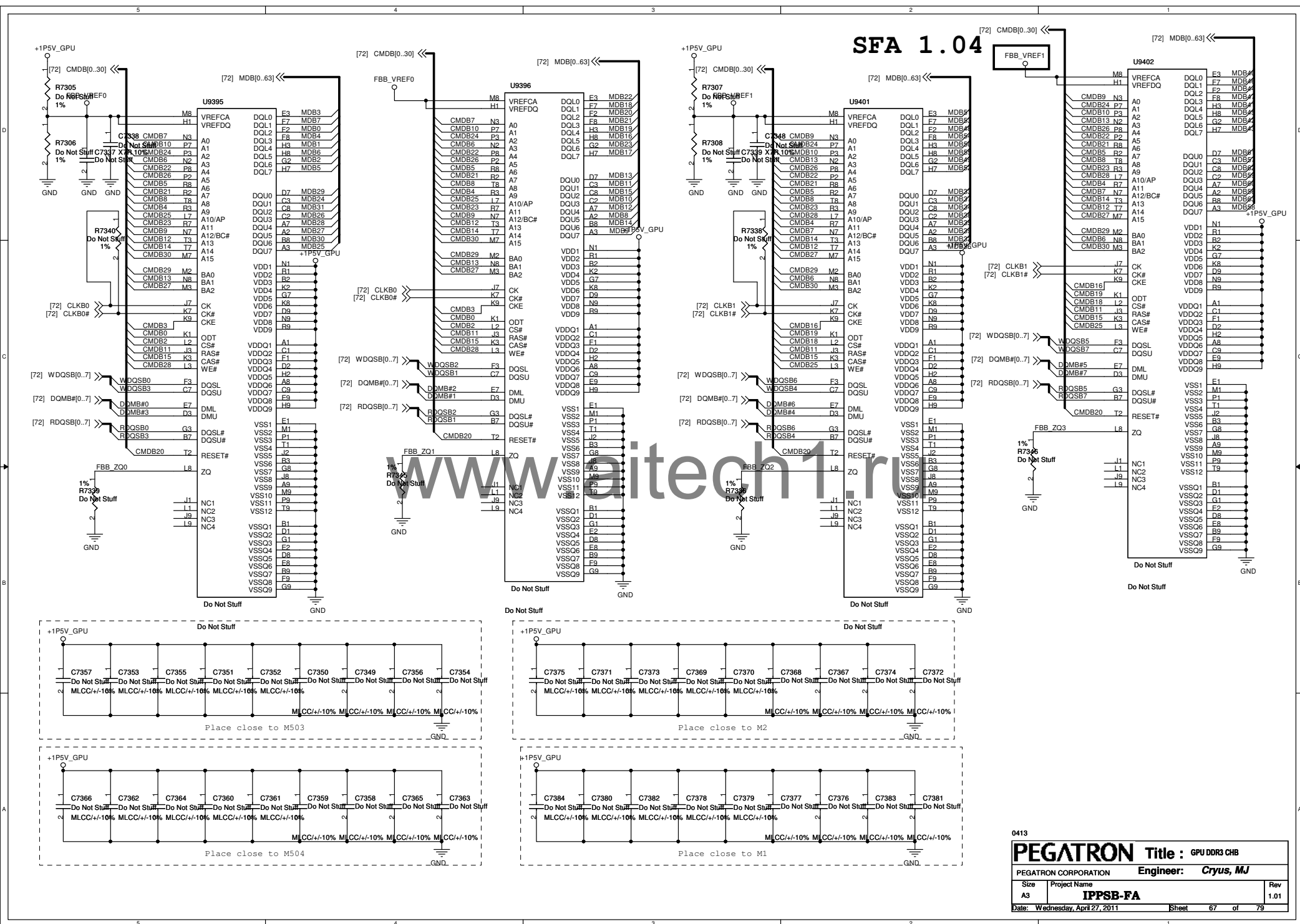
整份新增修改

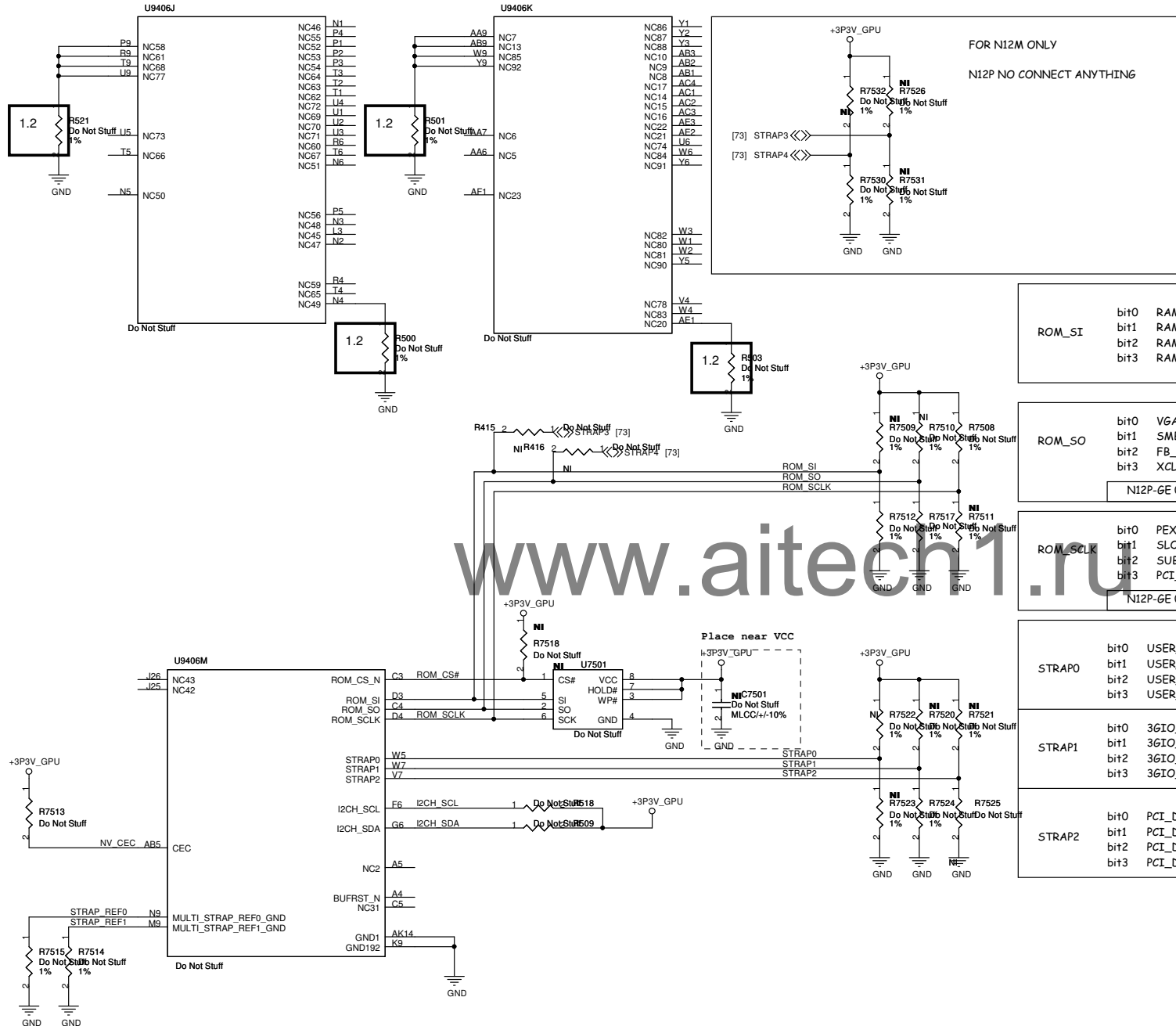
Install the VD1/VD2/VD3/VD4/VD5 diode to prevent from ESD issue

NOTE:









FOR NI2M ONLY
NI2P NO CONNECT ANYTHING

ROM_SI	bit0	RAM_CFG_0	1Gb (64Mx16 8pcs)
bit1	RAM_CFG_1	RAM_CFG[3:0] Definitions	
bit2	RAM_CFG_2	0x2: Hynix => H5TQ1663BFR-12C	
bit3	RAM_CFG_3	0x3: Samsung => K4W161646E-HC12	
0x0010 : 15K PD			

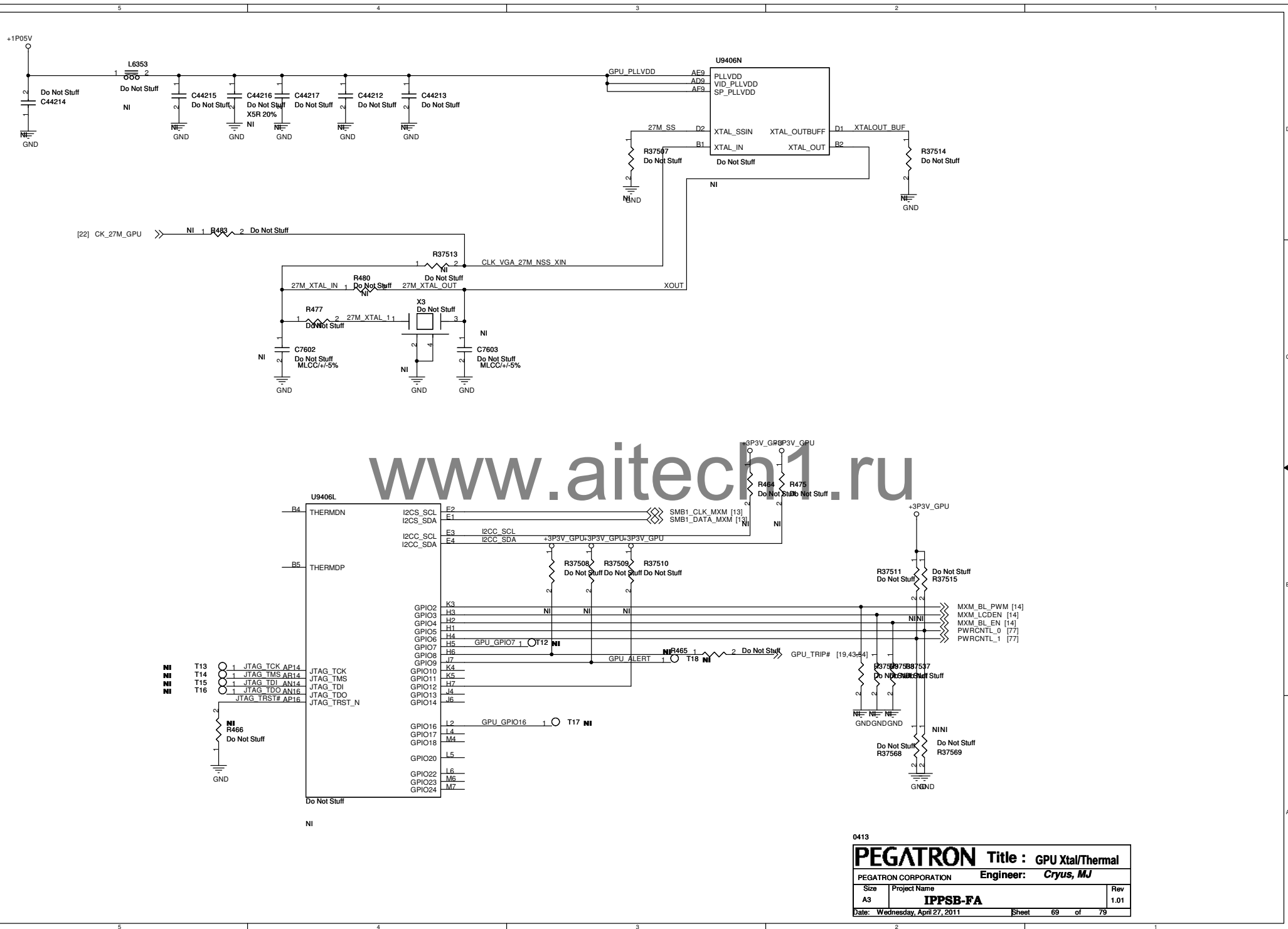
ROM_SO	bit0	VGA_DEVICE	1: VGA Device (default class code 300h)
bit1	SMB_ALT_ADDR	0: 0x9E (default)	
bit2	FB_O_BAR_SIZE	0: 256MB (default)	
bit3	XCLK_417	0: 277M Hz (default)	
NI2P-GE 0x0001 : 10K PD NI2M-GS 0x1001 : 10K PU different			

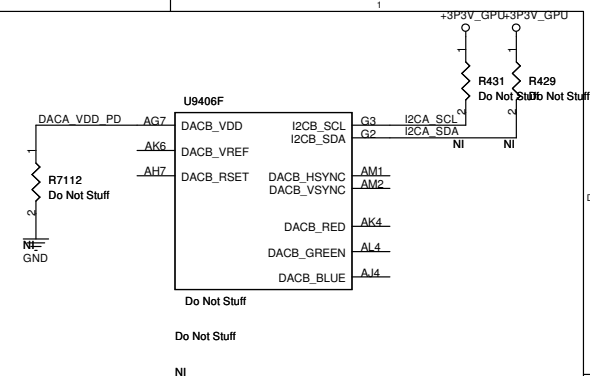
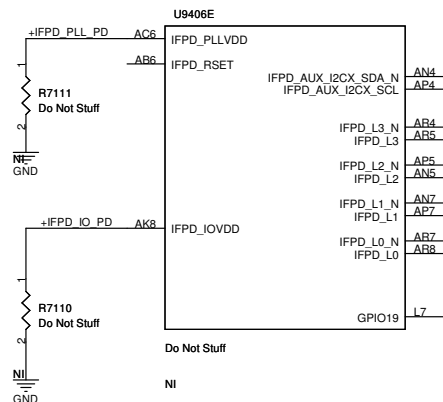
ROM_SCLK	bit0	PEX_PLL_EN_TERM	0: Disable (default)
bit1	SLOT_CLK_CONFIG <td>0: GPU & MCH not share common reference clock</td> <td></td>	0: GPU & MCH not share common reference clock	
bit2	SUB_VENDER <td>0: no vidio BIOS ROM</td> <td></td>	0: no vidio BIOS ROM	
bit3	PCI_DEVID_4 <td>1: PCI_Devid[4] => 0x0DFE bit 4 = 1</td> <td></td>	1: PCI_Devid[4] => 0x0DFE bit 4 = 1	
NI2P-GE 0x1110 : 35K PU NI2M-GS 0x1100 : 25K PU different			

STRAP0	bit0	USER_BIT0	0x0000 : 5K PD (Panels select Default 0x0000)
bit1	USER_BIT1		
bit2	USER_BIT2		
bit3	USER_BIT3		

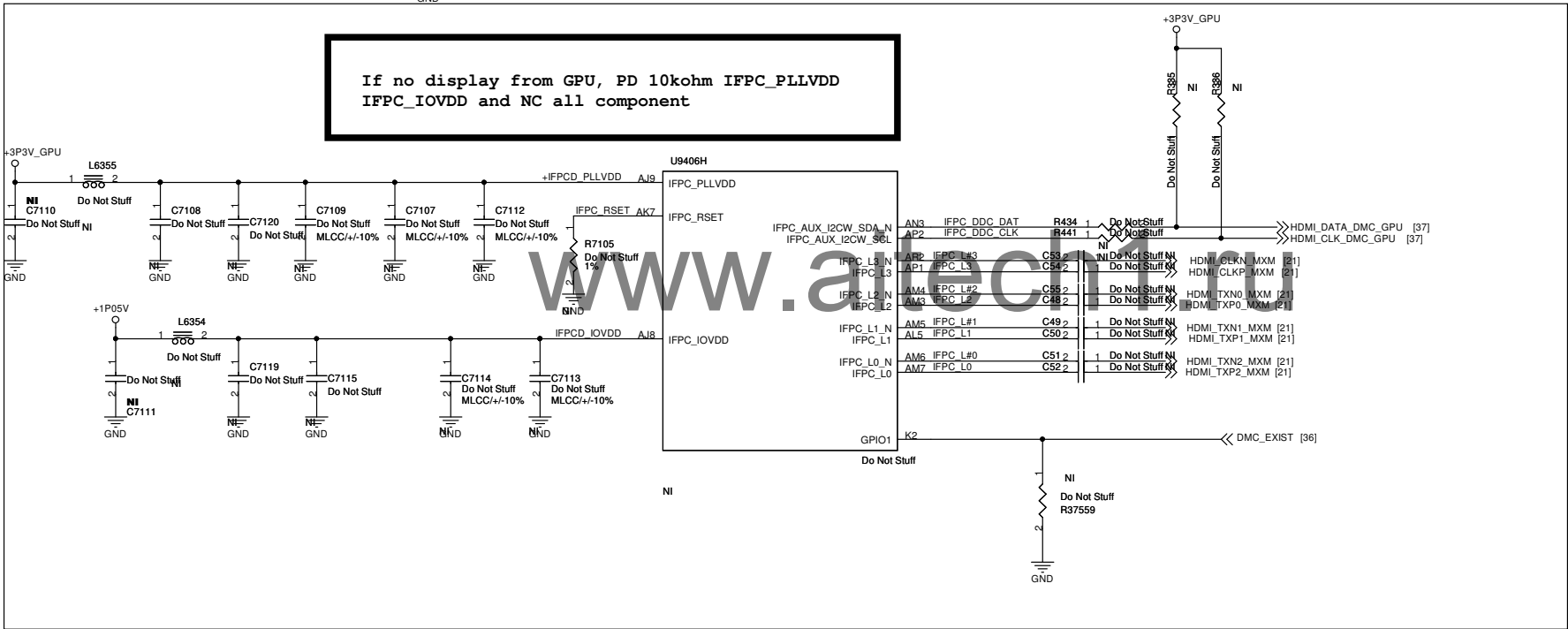
STRAP1	bit0	3GIO_PADC6_LUT_ADR0	0x6 : 35k PD (PCIE swing default)
bit1	3GIO_PADC6_LUT_ADR1		
bit2	3GIO_PADC6_LUT_ADR2		
bit3	3GIO_PADC6_LUT_ADR3		

STRAP2	bit0	PCI_DEVID_0	NI2P-GE 0x0101 : 30K PD NI2M-GS 0x0100 : 30K PD
bit1	PCI_DEVID_1		
bit2	PCI_DEVID_2		
bit3	PCI_DEVID_3		



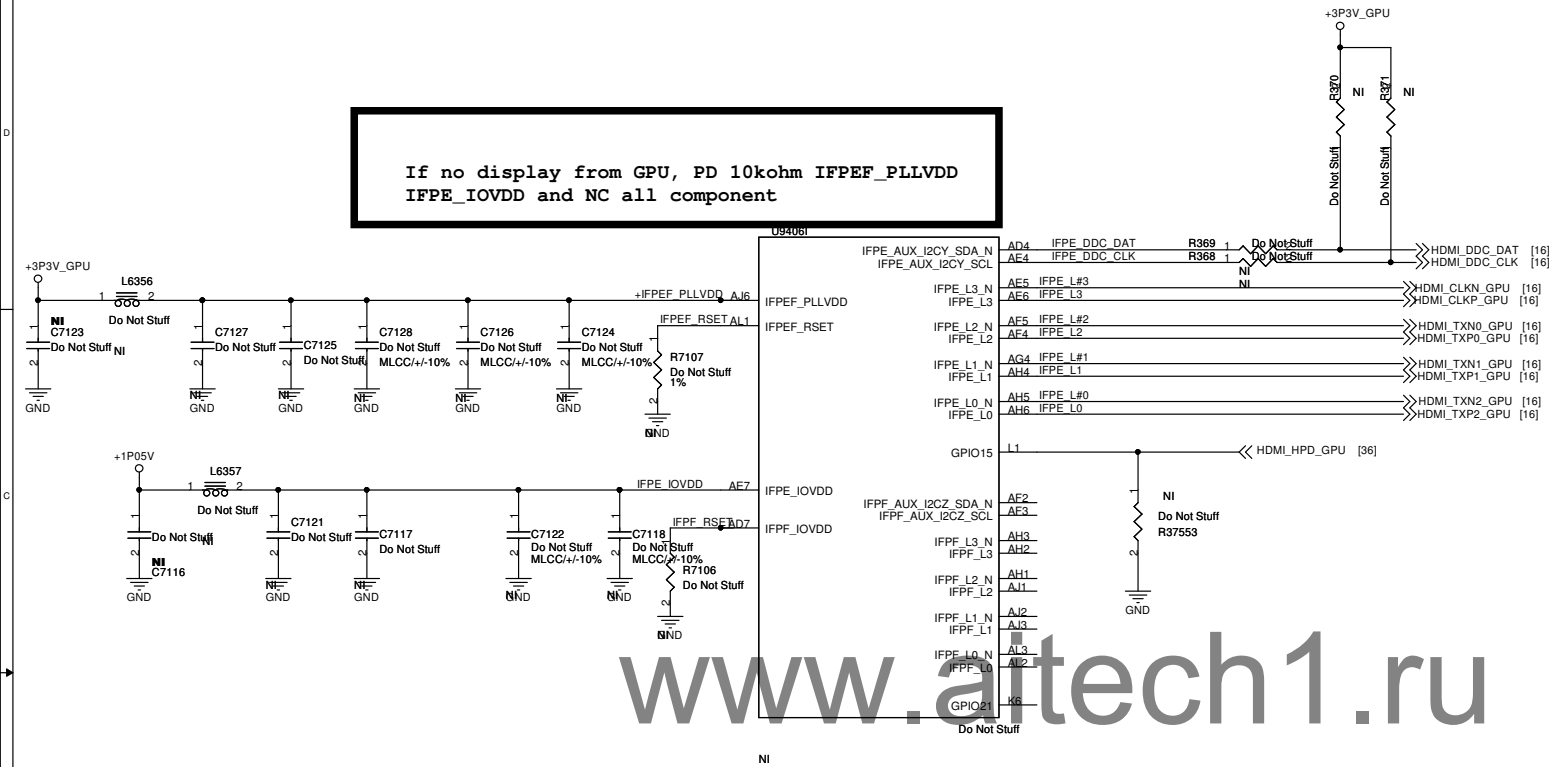


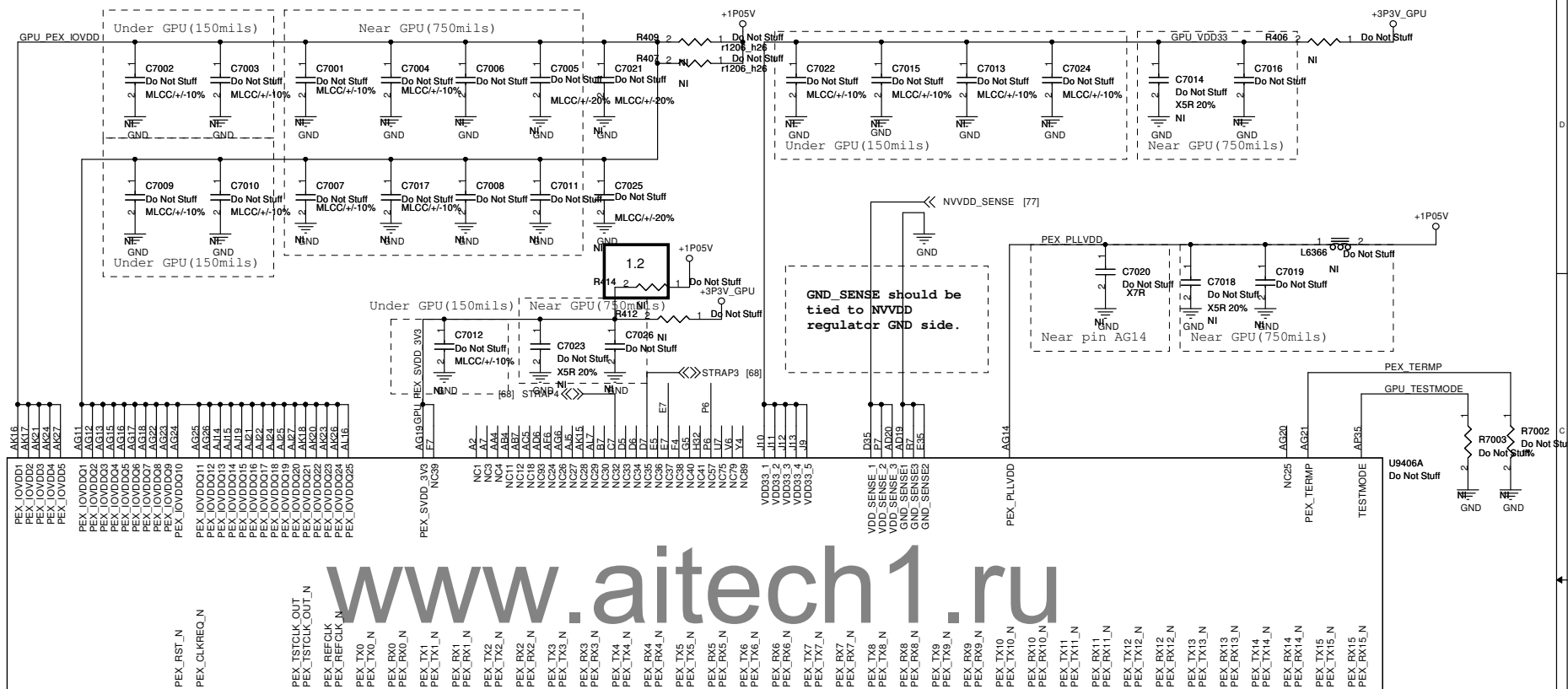
If no display from GPU, PD 10kohm IFPC_PLLVDD
IFPC_IOVDD and NC all component



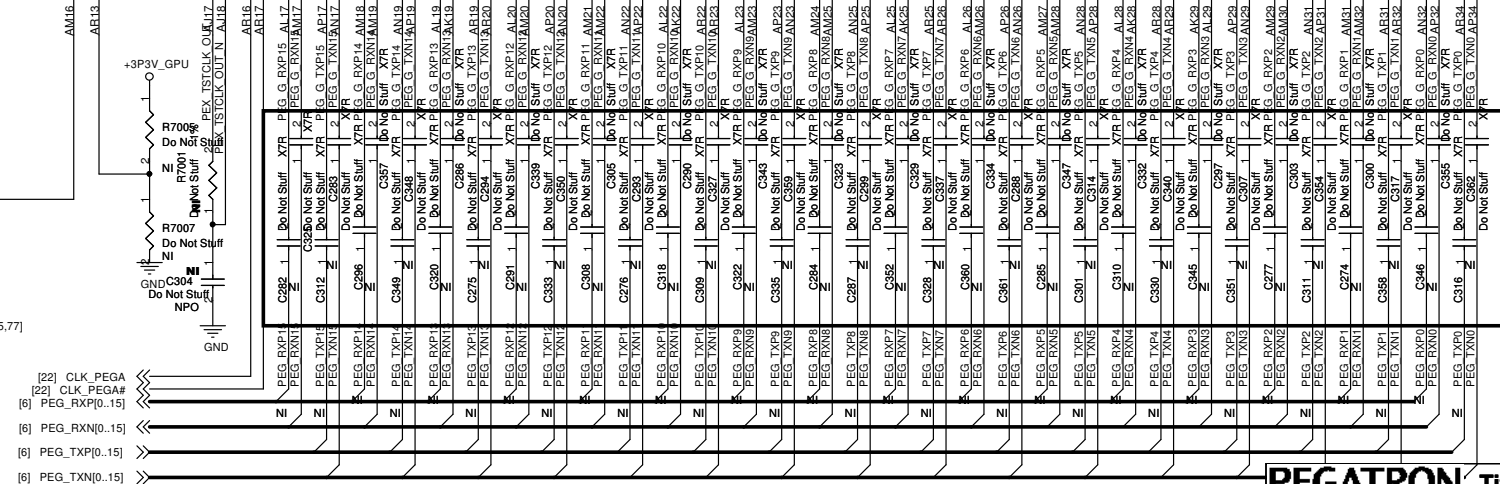
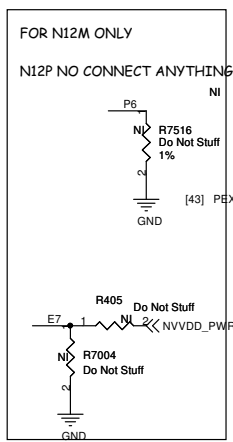
0413

If no display from GPU, PD 10kohm IFPEF_PLLVDD
IFPE_IOVDD and NC all component

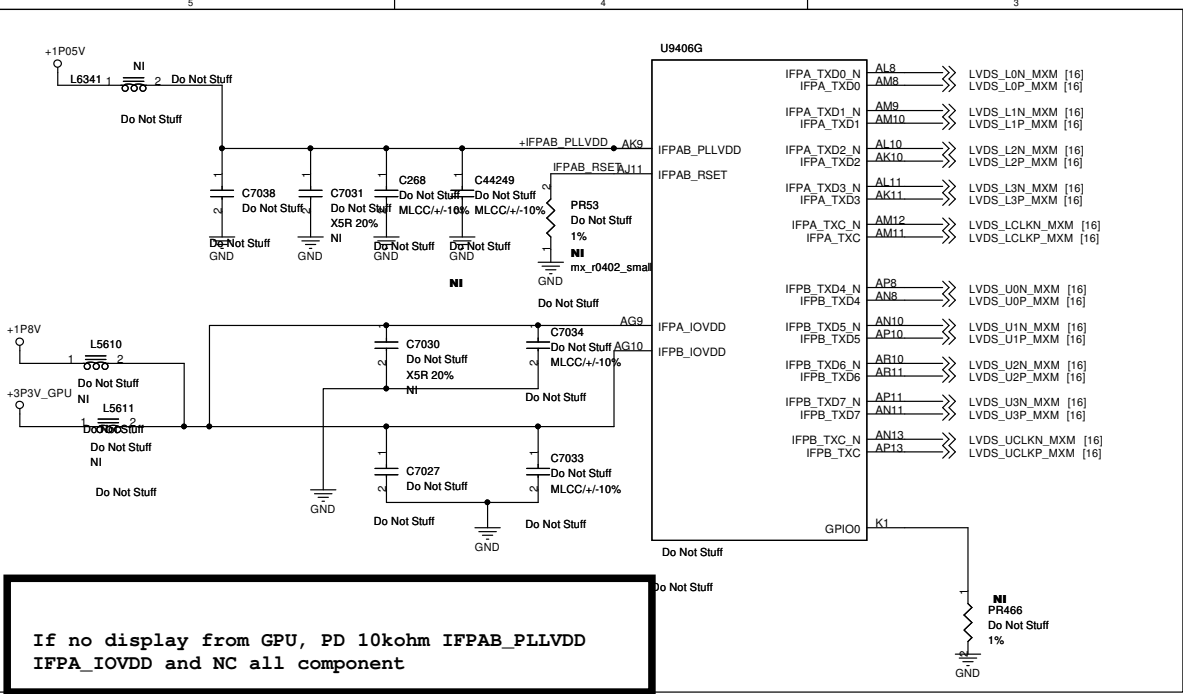




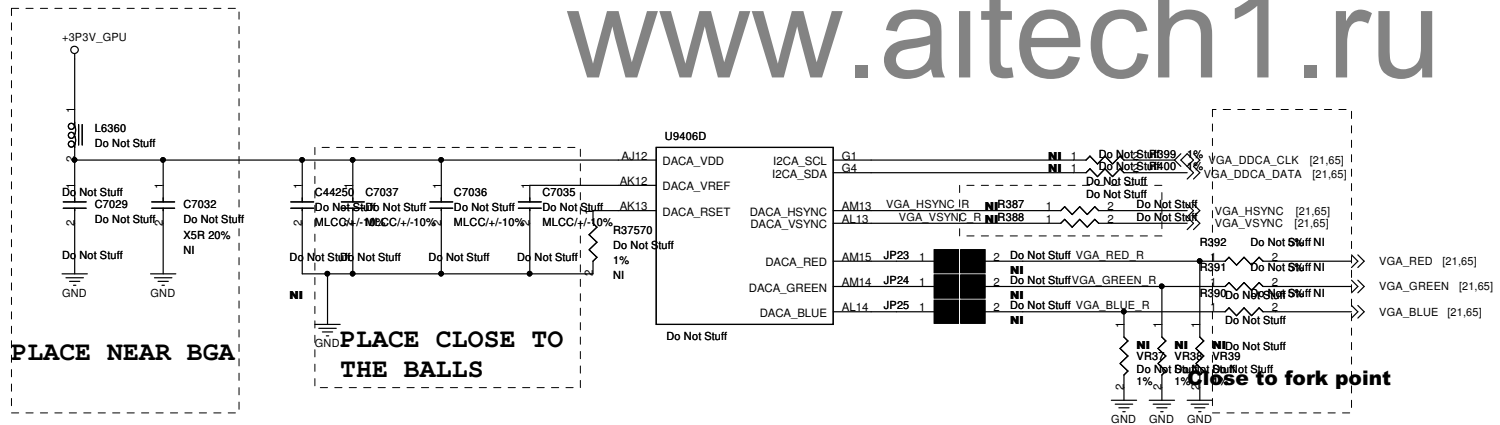
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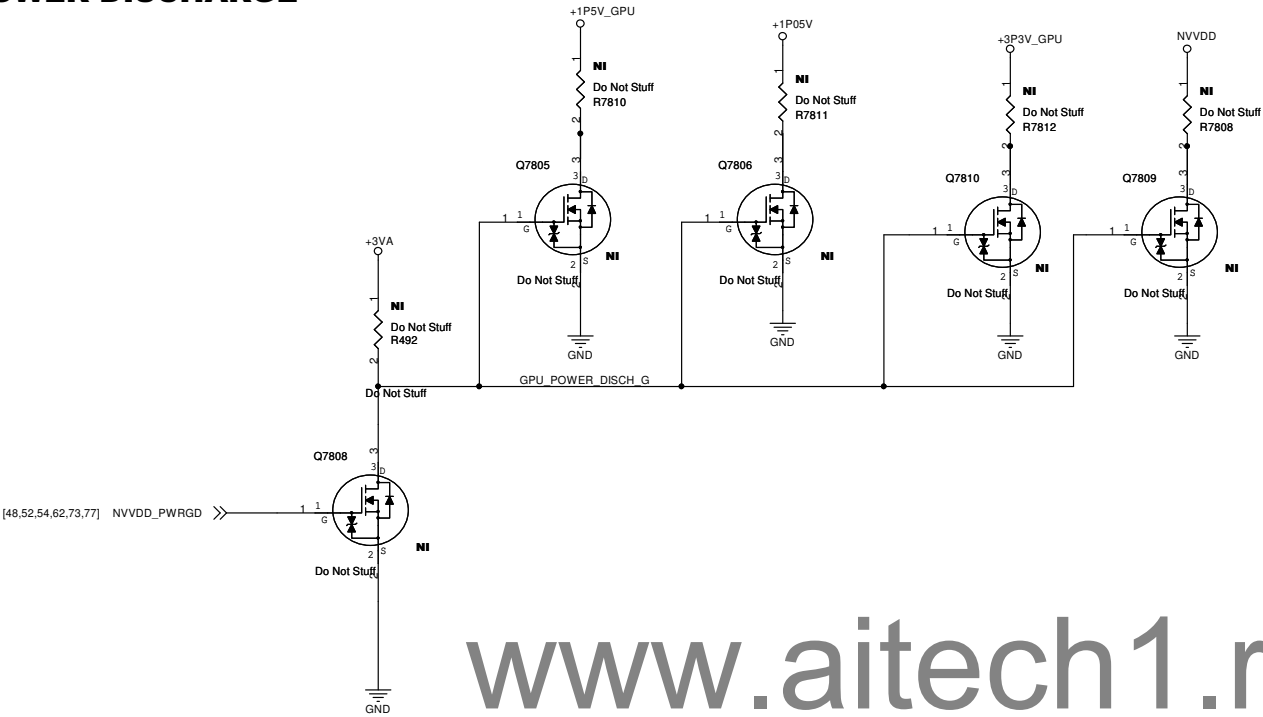
Rev 1.1



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GPU POWER DISCHARGE



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0413		
PEGATRON		
Title : GPU Discharge		
PEGATRON CORPORATION		
Engineer: Cryus, MJ		
Size	Project Name	Rev
A3	IPPSB-FA	1.01
Date: Wednesday, April 27, 2011		
Sheet 75 of 79		

U9406P	
AB11	VDD1
AB13	VDD2
AB15	VDD3
AB17	VDD4
AB19	VDD5
AB21	VDD6
AB23	VDD7
AB25	VDD8
AC11	VDD9
AC12	VDD10
AC13	VDD11
AC14	VDD12
AC15	VDD13
AC16	VDD14
AC17	VDD15
AC18	VDD16
AC19	VDD17
AC20	VDD18
AC21	VDD19
AC22	VDD20
AC23	VDD21
AC24	VDD22
AC25	VDD23
AD12	VDD24
AD14	VDD25
AD18	VDD26
AD18	VDD27
AD22	VDD28
AD24	VDD29
112	VDD30
113	VDD31
114	VDD32
115	VDD33
116	VDD34
117	VDD35
118	VDD36
119	VDD37
120	VDD38
121	VDD39
122	VDD40
123	VDD41
124	VDD42
125	VDD43
M12	VDD44
M14	VDD45
M16	VDD46
M18	VDD47
M20	VDD48
M22	VDD49
M24	VDD50
P11	VDD51
P13	VDD52
P15	VDD53
P17	VDD54
P19	VDD55
	VDD56
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	VDD111

